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1 GHz Current Mode Class-D Power Amplifier in Hybrid Technology Using GaN HEMTs

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Abstract. This paper presents the design and implementation of a highly efficient current-mode class-D (CMCD) power amplifier (PA) using commercial 2W GaN HEMT devices. A switchedbased model developed in-house for the GaN power device is used extensively for analysing and designing the 1 GHz CMCD PA in hybrid technology. The load coupling network, comprising a load transformation network, a higher harmonic impedance termination tank and a balun, measures only 3.7 cm×7.6 cm while providing suitable means for tuning the performance of the amplifier. The fabricated hybrid CMCD PA delivers an output power of around 36 dBm with an DC-to-RF efficiency of 65% over a wide frequency band.

Key words: Power amplifier, high efficiency, switching-mode, current-mode class-D PA, GaN HEMT.

1. Introduction

Linearity, efficiency and, hence, prime power consumption of a transmitter are mainly dominated by the performance of the power amplifier (PA). Conventional PAs like class A, AB, or B amplifiers are typically used for the transmission of spectral-efficient signals with a time-varying envelop. These classes provide linear or quasi-linear amplification but, when amplifying signals with large peak-to-average power ratios (PAPRs), efficiency of these circuits is notoriously low. By deliberately shaping current and voltage waveforms across the output terminal of the transistor so that

the overlap in time of high current and high voltage is minimised throughout the radio frequency (RF) cycle, switching-mode PAs achieve high efficiency also at microwave frequencies [1], [2]. However, because the device acts like a switch, these type of amplifiers are highly nonlinear and, thus, not suitable to replace conventional PAs in nowadays standard wireless transmitters. In order to obtain both good efficiency and high linearity, switching-mode PAs have to be employed in advanced transmitter architectures such as delta-sigma based transmitters, polar or envelope elimination and restoration (EE&R) and linear amplification using nonlinear components (LINC) [3].

Driving the transistor hard enough to mimic a switch and deliberately controlling the impedances at all higher harmonics result ideally in unity DC-to-RF efficiency. At RF and microwaves practical limitations for reaching efficiency of 100% are mainly the nonidealities of the transistor such as the saturation or knee voltage, ON-resistance, finite commutation time, as well as parasitic elements of the device and the load coupling network. Among the different switching-mode amplifier classes, class E, inverse F (F^{-1}) and current-mode class D (CMCD) have the advantage of providing zero voltage switching (ZVS). During the transition form the OFF- to the ON-state the voltage across the output terminal of the device is zero. If the voltage is nonzero, the energy E_C:

$$E_C = \frac{CV_{DC}^2}{2}, \tag{1}$$

stored in a parasitic capacitance or the energy E_L:

$$E_L = \frac{LI^2}{2}, \tag{2}$$

stored in a parasitic inductance is dissipated in each cycle.

With increasing switching frequency, these losses become more and more pronounced with deteriorating effects on efficiency. Since the loss due to charging and discharging of the output capacitance of the transistor increase with higher frequencies, zero voltage switching (ZVS) amplifiers provide better performance at microwave frequencies than their nonzero voltage switching counterparts.

This work reports design methodology using a switch-based model [4], implementation and measurement results of a CMCD PA in hybrid technology at 1 GHz. The physical dimensions of the load coupling network, as well as the component count were minimized by using a surface mount balun and microstrip load transformation networks.

2. Theory of operation

A current-mode class D power amplifier consists of two transistors working in push-pull configuration. Depending on the type of harmonic rejection circuit at the output, the amplifier can work in two different modes: if the LC-resonator is connected in series to the load and the bias is supplied via a constant voltage, the configuration operates in voltage mode. If the tank is connected to ground or placed between the outputs of the two devices and the bias is a constant current, the circuit will operate in current mode. Figure 1 shows a typical topology for realizing CMCD power amplifiers.

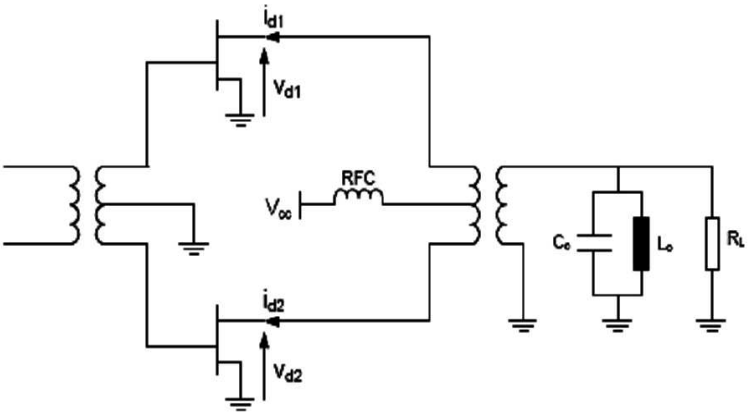

Fig. 1. Typical topology of a current-mode class D power amplifier.

As shown, the active devices operating in push-pull are driven by signals having the same amplitude but complementary phase components, i.e. the difference in phase is 180°. The push-pull structure removes even harmonics of the drain current by providing an open circuit at these frequencies, leading to half sinusoidal voltage waveform across the output terminal of the device. On the other hand the shunt tank, which is tuned to the fundamental frequency, shortens all odd harmonic frequency components to ground. The drain current is hence rich in odd harmonics and resulting in a square drain current waveform.

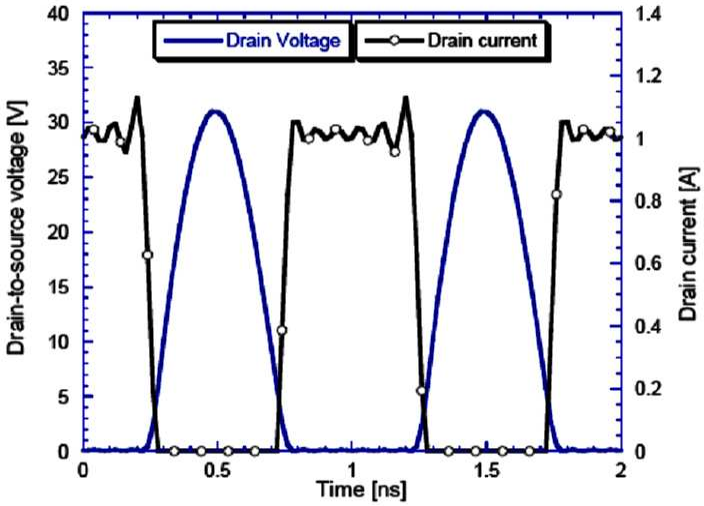

Fig. 2. Simulated ideal drain current and voltage waveform of one transistor in a CMCD PA.

Figure 2 shows ideal drain voltage and current waveforms at the output of one of the transistors of the CMCD PA topology shown in Fig. 1. The waveforms of the

second transistor are identical, except a phase shift of 180°. The product of drain current i_d and drain-to-source voltage v_{ds} of the waveforms shown in Fig. 2 is zero at all higher harmonics during the entire RF cycle, since the current only contains odd and the voltage only even harmonic components. Hence, the power dissipated in the device is ideally zero and DC-to-RF efficiency reaches unity.

3. Design and implementation

A. Large-signal device model

In this paper a highly efficient current-mode class D power amplifier is designed and simulated using the harmonic balance (HB) simulation tool of the advanced design system (ADS) software. Because of the unavailability of a suitable large-signal device model, a switch-based model according to [4] was extracted and implemented for the RT233 2W GaN HEMT from RFHIC. The developed model exploits the fact that assuming fast enough switching speed of the active device, the transistor spends most of the time in two discrete states, i.e. in the low-resistive ON- or in the highresistive OFF-state. Therefore, instead of extracting a fullfledged nonlinear model of the active device, a much simpler but still accurate model can be used. The proposed model, described in more detail in [4], contains a switch as the only nonlinear part of the transistor. The model is augmented by the most important extrinsic and intrinsic elements. The values of all model components can be easily extracted from small-signal S-parameter measurements of the device in a few specific bias points and form measured DC I-V curves. Figure 3 shows the block diagram of the used model implemented in Aglient ADS.

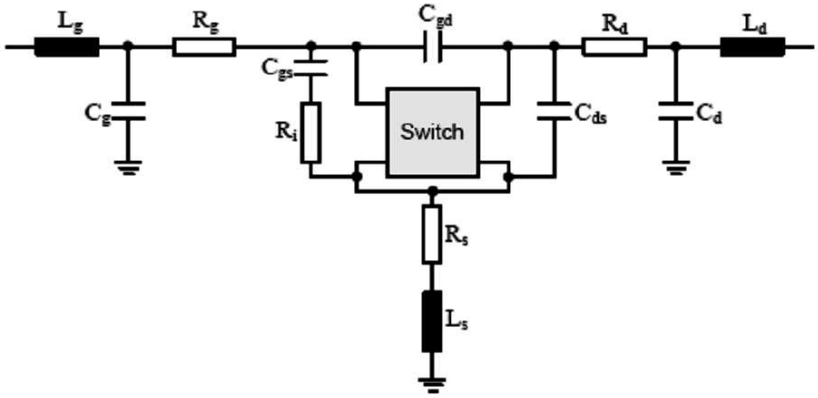

Fig. 3. Topology of the used switch-based GaN HEMT model. The model for the packaged device comprises a switch, which describes the behavior of the transistor, and the most important intrinsic and extrinsic elements which affect the performance in fast-switching applications.

B. Implementation details

Figure 4 shows the block diagram of the CMCD topology used in this work.

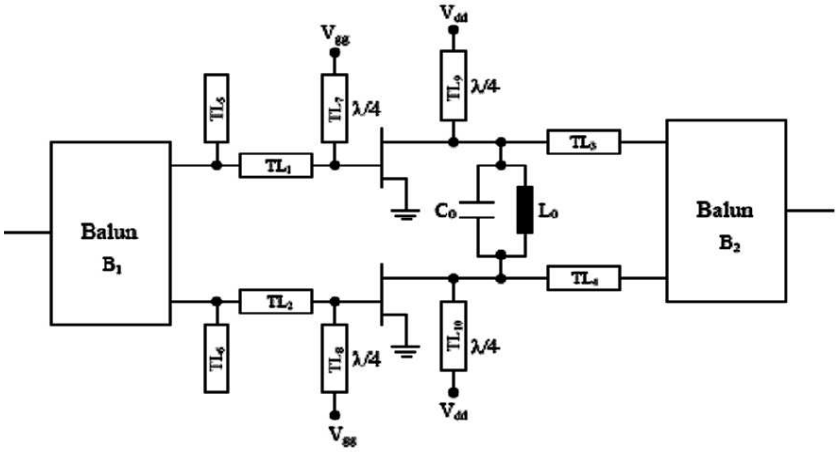

Fig. 4. Complete schematic of the proposed CMCD PA with compact load coupling network and surface mounted baluns.

In order to obtain two balanced signals from the singleended input terminal, the physically small surface mount device (SMD) Xinger 3A425 balun from Anaren was used.

The balun provides a convenient impedance transformation from single-ended 50 Ω to single-ended 25 Ω in the frequency band of operation. To combine the output of the two transistors to a single-ended 50 Ω terminal, the same SMD balun is used. The parallel-tuned tank $L_0 - C_0$ in Fig. 4, which is attached across the output of the two power transistors, is realised with a discrete ceramic SMD capacitor form ATC and an air-wound inductor. Part of the output capacitance of the packaged GaN transistors was absorbed into C_0 and the value of C_0 lowered accordingly. The right amount of inductance is provided by an air-wound inductor instead of using an electrically short transmission-line [5], [6]. The network was fabricated on a Rogers RO5870 508 μm-thick substrate. The performance of the circuit at the odd harmonics can be tuned by varying the capacitance value C_0 and by manipulating the air-wound inductor accordingly. The impedance at the fundamental frequency is close to 25 Ω for the selected device.

Fine-adjustment can be done through small changes of the drain supply voltage V_{DC}. The total physical size of the load coupling network, including quarter wave biasing lines, is 37 mm×76 mm. Compact output networks are generally an asset in highly efficient PAs, as resistive loss in the high power side is kept low.

In order to maximize gain and, thus, power added efficiency (PAE), the input matching network was designed to transform the 25 Ω output impedance of the balun down to the complex conjugate impedance of the devices. However, due to the reduced accuracy of the switched-based model in describing the input behavior of the device, various tuning possibilities were incorporated.

Figure 5 shows the photograph of the fabricated CMCD PA mounted on a heat-sink and connectorised.

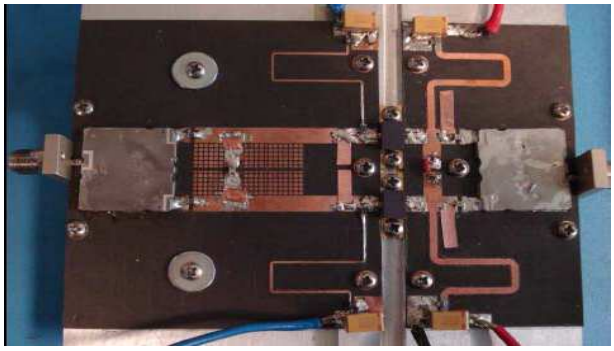

Fig. 5. Photograph of the manufactured highly efficient 1 GHz CMCD PA. The size of the entire PA module is 76 mm×107 mm.

4. Experimental results

Unless indicated differently, all large-signal measurements were taken with both devices biased at a gate-to-source voltage $V_{GS} = -2.2$ V and a drain-to-source voltage $V_{DC} = 10$ V.

Figure 6 shows the measured gain G and output power P_{out} of the amplifier versus input power P_{in}.

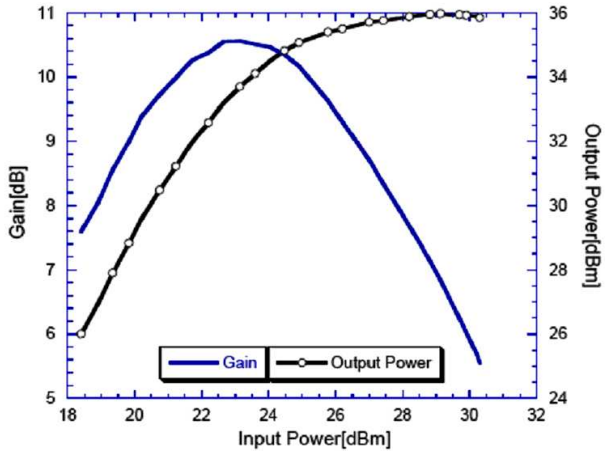

Fig. 6. Measured output power and gain of the manufactured CMCD PA biased at $V_{DC} = 10$ V and $V_{GS} = -2.2$ V at 1 GHz.

Measured G is more than 7 dB for drive levels up to 29 dBm with a peak of 10.6 dB at $P_{in} = 23$ dBm. Output power of the CMCD amplifier at 1 GHz saturates at

36.0 dBm for a P_{in} of 29 dBm. At these power levels, peak drain efficiency h = 65.1% is recorded as shown in Fig. 7.

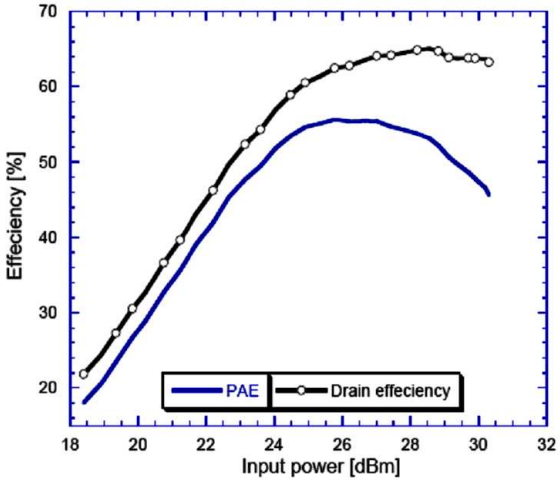

Fig. 7. Measured drain and power added efficiency of the 1 GHz class D PA biased at V_{DC} = 10 V and V_{GS} = –2.2 V.

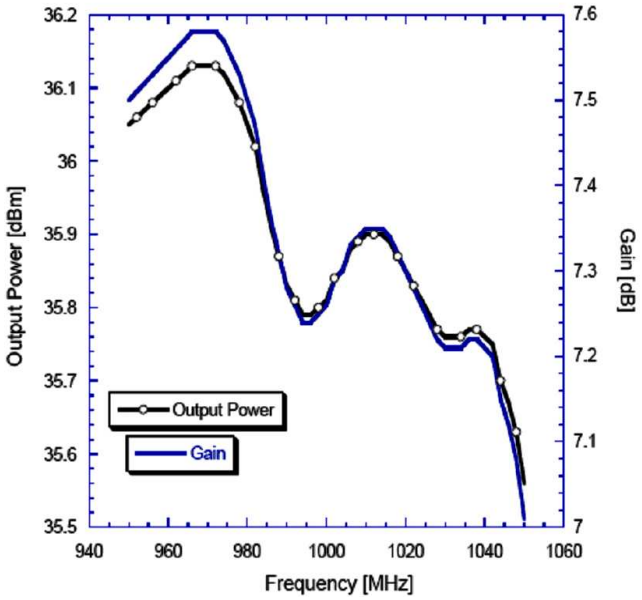

Fig. 8. Measured gain and output power of the CMCD PA over a 100 MHz bandwidth at a constant drive level of 29 dBm.

For larger drive levels, h remains almost constant. However, due to the high gain compression of the devices, PAE of the CMCD amplifier is low at these power

levels. For instance, at peak drain efficiency, the devices are more than 3 dB into gain compression and the measured PAE is 53%. Maximum PAE of 55.8% is achieved at $P_{in} = 26.0$ dBm and an output power of 35.5 dBm.

Figure 8 shows measured G and Pout of the CMCD PA versus frequency. For a constant input drive level of 29 dBm, i.e. the same input power as in Fig. 7, output power and gain peak at 0.97 GHz and 1.01 GHz to 36.13 dBm and 35.9 dBm, respectively. As it can be seen in Fig. 8, the output power of this amplifier changes by less than 0.6 dB over a 100 MHz bandwidth.

Gain of this amplifier has also two peaks in 7.6 dB and 7.35 dB at the same frequencies as output power does. Similarly, gain changes around 0.6 dB all over the 100 MHz bandwidth.

Figure 9 shows h and PAE performance of the PA from 0.95 GHz to 1.05 GHz. Drain efficiency and PAE peak at 66% and 54.5%, respectively. The two maximas occur again at 0.97 GHz and 1.01 GHz. As it is shown in this figure the variation of both drain and power added efficiency is around 5% in the measured frequency band.

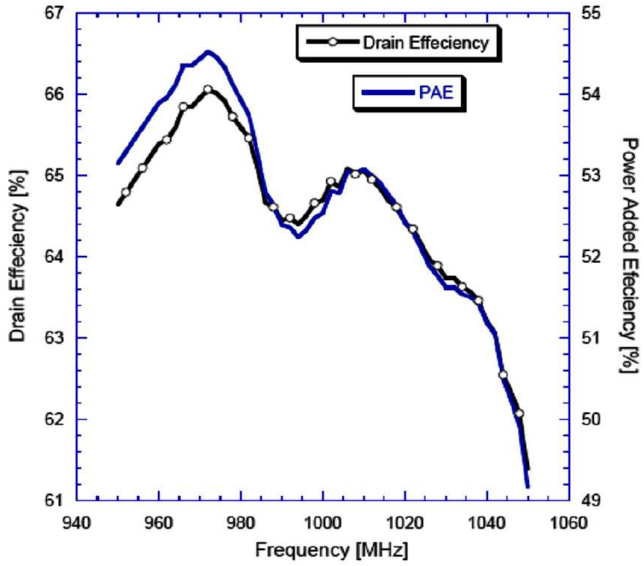

Fig. 9. Drain and power added efficiency of the manufactured PA versus frequency driven at 29 dBm.

Measured output power for different values of drain supply voltage V_{DD} is shown in Fig. 10. For drain voltages between 5 V and 15 V output power is linearly proportional to the applied drain supply voltage V_{DD}. For V_{DD} greater than 15 V the output power levels off. Nonlinearity of output power versus V_{DD} of the CMCD PA for low supply voltages is because of drive power leakage from the input to the output of the amplifier. At low drain bias voltages output power of the devices is low. However, portion of the strong input power appears at the output. Due to this leakage, the reduction in Pout is distorted for decreasing V_{DD} and approximates a minimum determined by the input-to-output isolation of the device and the circuitry around it.

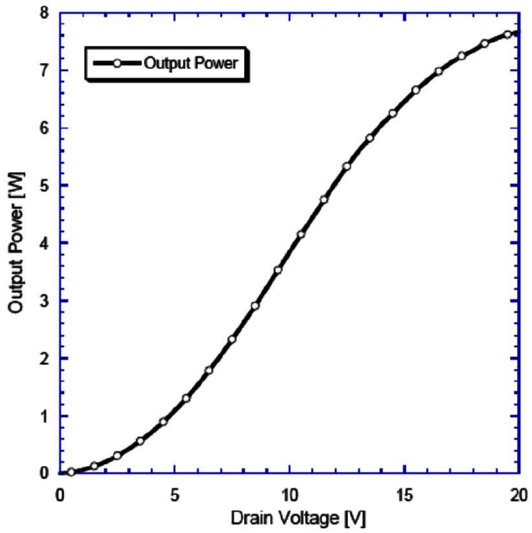

Fig. 10. Measured Pout as function of the drain supply voltage of the PA when driven at 29 dBm.

Figure 11 shows h and PAE of the amplifier as function of the drain bias voltage. While measured PAE is highest for supply voltages around the nominal value of $V_{DD} = 10$ V with a peak at 54.0% at 11.4 V, eta is highest for low supply voltages and decreases as drain bias voltage increases. Again, the stronger contribution of drive power leakage to total output power of the circuit with lower supply voltage is the main cause for the trend.

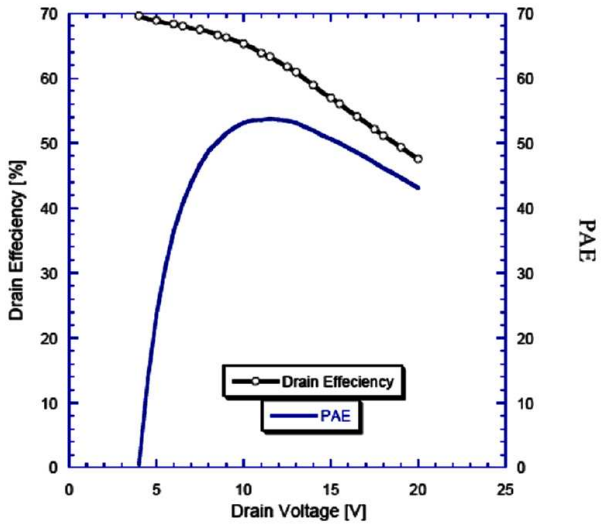

Fig. 11. Drain and power added efficiency for varying V_{DD} and a constant input drive level of 29 dBm.

5. Conclusion

A hybrid current-mode class-D power amplifier has been designed with a compact sized load-coupling network using an in-house developed switch-based transistor model. The size of the manufactured output network is 37 mm×76 mm. The manufactured CMCD PA achieves an efficiency of 65.4% for an output power of 36.0 dBm and a large-signal power gain of more than 7 dB around 1 GHz. Measured power added efficiency and output power are more than 50% and 35.5 dBm over a 100 MHz bandwidth. The linear dependency of output power form the applied drain supply voltage makes this type of amplifier suitable for applications in both polar and envelope elimination and restoration based transmitters.

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