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Current Sensing Accuracy Improvement by Feedback Offset Cancelation

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Abstract. This paper presents a precision over current protective function integrated in a high side power switch. The accuracy improvement is based on using a low offset, autozero amplifier for providing the same bias conditions for both the power and the sense transistors.

Key-words: high side switches, current protection.

1. Introduction

Integrated switches tend to replace the classical relays in an increasing range of applications. The main advantage of the integrated solutions is the possibility of integrating the driving and protection functions together with the actual switch, making the power device control much easier and increasing the application robustness.

A critical function is the protection against short circuit conditions. Many topologies have been implemented for measuring the load current and protecting the active device, either by switch-off or current limitation. [1] The circuit accuracy and complexity vary with the application requirements. Higher sensing accuracy is generally needed for load diagnosis. This paper focuses on a precision over current protection function integrated in a high side switch.

2. Current Sensing Topologies

In automotive applications, switches are used to connect different loads types to the car battery. Load types vary from LED and relays to bulbs and d.c. motors,

resulting in a wide range of required switch currents and resistances. An important requirement is that the switch protects itself against any system malfunction.

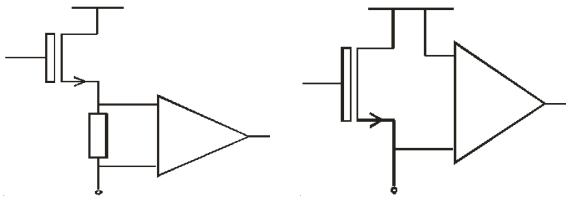

Fig. 1. Direct current measurement topologies.

The switch can be connected between load and ground, commonly referred to as *low side switch*, or between supply and load, respectively referred to as *high side switch*. In this paper, we only present the high side current sensing topologies, but they can easily be adapted to low side switches as well.

A switch (in *on* state) is basically a resistor, so the power it dissipates is equal to the square load current multiplied by its on state resistance $P = R_{on}I_L^2$. As the load current increases, the on state resistance must be reduced to limit the dissipated power. As we move to higher current applications, the allowed switch voltage drop becomes smaller.

In this section we discuss the changes suffered by the current sensing circuit in order to adapt to the reduced switch voltage drop.

The easiest current sense method is to insert a sense resistor in the current path and than measure the resulting voltage drop. This topology is presented in Fig. 1(a). The main drawback of this solution is that the sense resistance is added to the total switch on state resistance, at is it connected in series with the actual switch. Even for moderate resistance switches, additional solutions must be searched.

A possible approach is presented in Fig. 1(b). In this case the switch is used as a "sense resistor" as well. We measure the switch voltage drop and, based on it, we estimate the load current. This solution implies no additional resistance in the load current path and is quite easy implemented. However, the switch on state resistance varies dramatically with temperature, process variation and supply voltage, making this approach inaccurate.

Most current measuring topologies do not measure directly the output current but use a sense transistor to conveniently "mirror" and "scale down" this current. Such a topology is presented in Fig. 2(a). A sense transistor is connected in parallel to the power switch and ideally its current is given by the output current divided by the geometric ratio between power and sense transistors.

The sense resistor is connected in parallel to the sense transistor. As the sense current is typically much lower then the output current, reasonable sense resistor values can be used. We note that the sense transistor and resistor are connected in parallel to the switch so they do not increase the total output resistance.

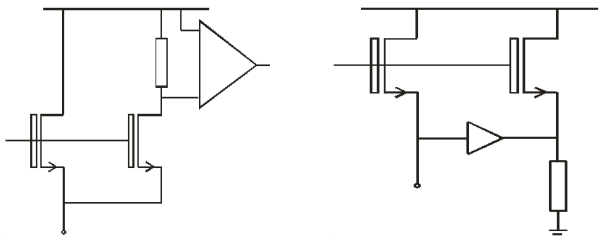

Fig. 2. Sense transistor current measurement topologies.

We note that the voltage drop across the sense resistor appears as a mismatch between power and sense transistors. This mismatch affects the mirroring accuracy, so the voltage drop across the sense resistor must be small compared to the switch voltage drop. For very low resistive switches, this condition cannot be fulfilled.

This problem is solved by the topology presented in Fig. 2.(b). The sense transistor voltage drop is controlled by a buffer that matches it to the power transistor. For this configuration, the output and sense current paths are independent, and the sense resistor voltage drop does not influence the mirroring accuracy.

3. Over Current Detection

The output current measuring topology used in this paper is presented in Fig. 3. [2] A sense transistor, M_2, is added in parallel to the main power switch, M_1, for mirroring a sense current, I_{sense}, that is then compared to a threshold.

M_1 and M_2 have their gate and drain connected together. Amplifier A_1 forces the source voltages of both transistors to be equal. As a result, transistors M_1 and M_2 are virtually connected in parallel, so the current densities are equal. The ratio between the output and sense current is then given by the multiplicity ratio:

$$I_{load} = K_{ILIS} I_{sense}, \tag{1}$$

where typical K_{ILIS} value is between 100 and 10 000, depending on power transistor size.

The sense current is converted in a voltage, by applying it on a sense resistor, R_{sense}, and then compared with a reference voltage, V_{ref}.

$$V_{sense} = I_{sense} R_{sense}. \tag{2}$$

A trimmed reference current is used to generate the comparison voltage, V_{ref}, on a reference resistance, R_{ref}, matched with the R_{sense}.

When the load current crosses a certain threshold, the sense voltage becomes higher than the reference, so A_2 comparator signals over current conditions. The threshold condition is:

$$V_{sense} = I_{sense} R_{sense} = I_{ref} R_{ref} = V_{ref}. \tag{3}$$

The threshold output current results:

$$I_{load} = K_{ILIS} \frac{R_{ref}}{R_{sense}} I_{ref}. \tag{4}$$

This equation highlights the factors influencing current sensing accuracy: the power to sense transistors ratio, K_{ILIS}, the R_{ref}/R_{sense} ratio and the reference current I_{ref}. Integrated resistors can be matched with accuracy below 1%, so R_{ref}/R_{sense} ratio is not a major concern for the overall accuracy. A typical integrated current source has a spread of about 20% to 30%, so for precision current detection current trimming is required.

The K_{ILIS} ratio has the biggest impact on current sensing accuracy, as the two matched devices have completely different size and geometry, typically work at different temperatures and the matching between power devices is generally poor (compared to low voltage devices).

This paper focuses on presenting a circuit technique for providing the same "bias condition" for the power and sense transistors, to achieve the best K_{ILIS} accuracy, and consequently, a better current sensing accuracy.

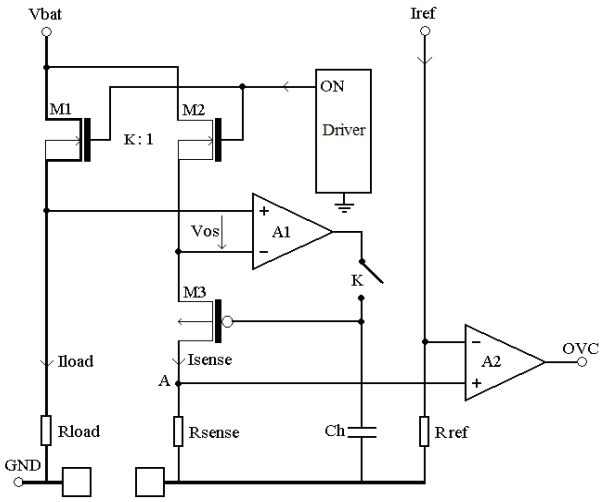

Fig. 3. Over current detection.

4. The A_1 amplifier offset effect

For accurate sense current mirroring, transistors M_1 and M_2 should have the same source voltage. These source voltages are kept constant by the feedback loop controlled by the A_1 amplifier. The amplifier offset voltage appears as a mismatch between the two sources voltages, resulting in a sense current error.

In this section we develop an analytical model for the A_1 amplifier offset voltage influence on sense current mirroring precision.

For both, power and sense transistors, we use the linear region model:

$$I_{load} = K_{load} \cdot \left[(V_{GS,load} - V_T) \cdot V_{DS,load} - \frac{V_{DS,load}^2}{2} \right], \tag{5}$$

$$I_{sense} = K_{sense} \cdot \left[(V_{GS,sense} - V_T) \cdot V_{DS,sense} - \frac{V_{DS,sense}^2}{2} \right]. \tag{6}$$

The A_1 amplifier offset affects both the gate-source and drain-source voltages. However, the gate-source voltage is much larger than the offset voltage so we can consider the two gate voltages equal in a first approximation.

$$V_{GS,load} = V_{GS,sense},$$
$$V_{GS,load} - V_T = V_{GS,sense} - V_T = V_{OV}. \tag{7}$$

We take into account the offset voltage mismatch between power and sense transistors drain-source voltages.

$$V_{DS,load} = V_{DS,sense} + V_{os}. \tag{8}$$

We use the output to sense current ratio (K_{ILIS}) to measure the sense current accuracy. From equations (5), (6) and (7) we get:

$$K_{ILIS} = \frac{I_{load}}{I_{sense}} = \frac{K_{load}}{K_{sense}} \cdot \frac{V_{OV} \cdot V_{DS,load} - V_{DS,load}^2/2}{V_{ov} \cdot V_{DS,sense} - V_{DS,sense}^2/2}. \tag{9}$$

Also taking into account equation (8), we get the current ratio expression of the two transistors depending on the amplifier's offset voltage.

$$K_{ILIS} = \frac{K_{load}}{K_{sense}} \cdot \frac{1}{1 - \dfrac{V_{OV} \cdot V_{os} - V_{DS,load} \cdot V_{os} + V_{os}^2/2}{V_{OV} \cdot V_{DS,load} - V_{DS,load}^2/2}}. \tag{10}$$

As V_{os} and $V_{DS,load}$ are very small, we can neglect the second order effects, resulting in:

$$K_{ILIS} = \frac{I_{load}}{I_{sense}} = \frac{K_{load}}{K_{sense}} \cdot \frac{1}{1 - V_{os}/V_{DS,load}}. \tag{11}$$

This result shows that the K_{ILIS} accuracy is determined by the power and sense transistor matching (described by K_{load}/K_{sense}) and by the A_1 offset voltage induced error. For achieving a high K_{ILIS} accuracy, the $V_{os}/V_{DS,load}$ ratio should be reduced as much as possible.

The voltage $V_{DS,load}$ is given by the *on* state resistance multiplied by the current threshold, so the $V_{os}/V_{DS,load}$ ratio can only be reduced by decreasing the offset. We also note that the offset error is more important at detecting lower currents, when $V_{DS,load}$ is smaller.

5. K_{ILIS} dependence on output current level

In some applications, it is needed to measure the current level, not only detect a specific current threshold. The A_1 amplifier offset voltage introduces a K_{ILIS} ratio dependence on the power transistor drain – source voltage, as given by equation (11). At high current levels, the voltage drop on the power transistor is also higher, making the offset voltage induced error negligible. As the load current decreases, the $1–V_{os}/V_{DS,load}$ term contribution becomes more important.

The K_{ILIS} accuracy dependence on output transistor drain – source voltage is presented in Fig. 4. We considered a given, process induced, mismatch between the power and sense transistor (independent on applied drain – source voltage). This process mismatch is multiplied by the offset induced error determined in the previous section.

The maximum and respectively minimum K_{ILIS} ratios are given by:

$$K_{Max} = \frac{K_{id}(1+\alpha)}{K_{id}} \cdot \frac{1}{1 - V_{os}/V_{DS,load}}, \tag{12}$$

$$K_{Min} = \frac{K_{id}(1-\alpha)}{K_{id}} \cdot \frac{1}{1 - (-V_{os})/V_{DS,load}}, \tag{13}$$

where K_{id} is the ideal K_{ILIS} ratio, given by the power to sense transistors geometry ratio and α is the technological maximum K_{ILIS} spread. We have considered the worst case offset voltage for each case ($+V_{os}$ for K_{Max} and $–V_{os}$ for K_{Min}).

From Fig. 4 we can see that, at high $V_{ds,load}$ values, the offset error contribution is negligible and the K_{ILIS} deviation is given by the technology mismatch, α. For the lower $V_{ds,load}$ range, the offset voltage contribution increases the total K_{ILIS} error.

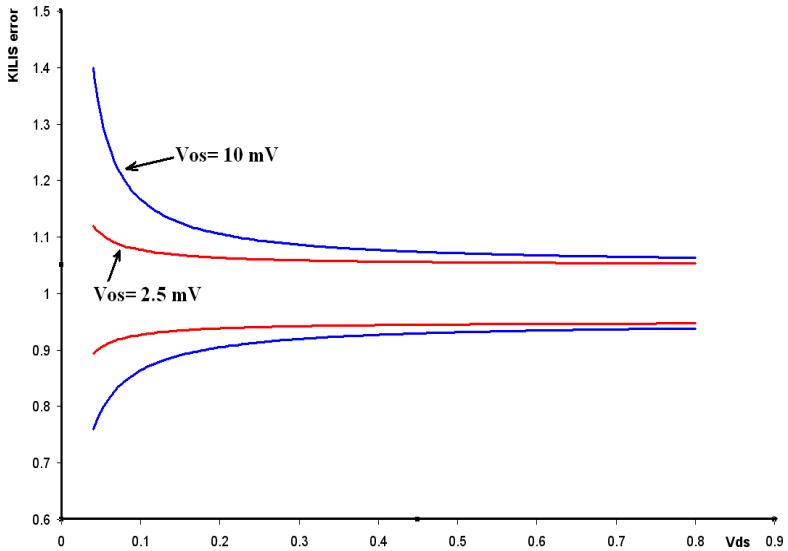

Fig. 4. K_{ILIS} accuracy dependence on output transistor drain – source voltage.

As a rule, we consider the offset error negligible for a minimum $V_{ds,load}$ voltage at least ten times larger than the V_{os}. The minimum output current that does not introduce significant K_{ILIS} error is:

$$I_{load,\min} = 10 \ \frac{V_{os}}{R_{DS,on}}. \tag{14}$$

We compared the K_{ILIS} error introduced by two different offset voltage levels. A lower offset voltages means that the offset voltage error will be negligible for a lower $V_{ds,load}$.

6. Autozero Amplifier Implementation

For obtaining an optimal current mirroring accuracy, the A_1 amplifier offset voltage is reduced using the autozero technique. In this section, we present the amplifier topology and estimated residual offset. [3, 4]

The autozero technique works in two phases: *sampling phase* and *signal processing phase*.

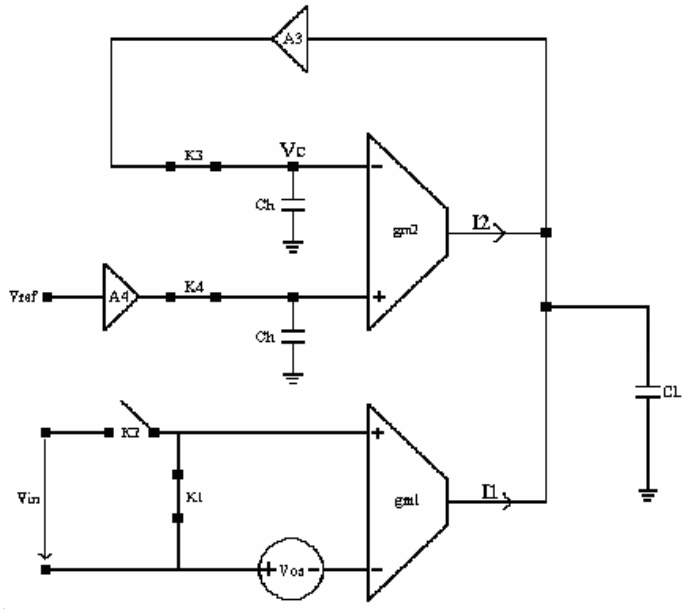

Fig. 5. The autozero topology.

During the *sampling phase,* the switches K_1, K_3 and K_4 are *on* and the switch K_2 is *off*. During this phase, the g_{m1} stage input voltage is its offset voltage, V_{OS1}. Due to g_{m2} and A_3 negative compensation loop action, the output voltage is driven to zero by developing on the hold capacitor the compensation voltage, V_C. At the end of the sampling phase, by turning *off* the switch K_1, the appropriate compensation voltage

that produces a zero voltage output for a zero differential input signal is stored on C_h capacitor.

The circuit then switches to the signal processing phase. The amplifier is connected to the signal path and the correction voltage sampled during the previous phase is applied on the negative input of the correction amplifier.

Based on circuit operation equations:

$$I_1 = g_{m1} V_{OS\,1}, \tag{15}$$

The current I_2:

$$I_2 = g_{m2} \cdot (A_4 \cdot V_{ref} - V_C), \tag{16}$$

The output voltage:

$$V_o = R_L \left(I_1 + I_2\right), \tag{17}$$

The compensation voltage:

$$V_C = A_3 V_o, \tag{18}$$

The compensation voltage results:

$$V_C = \frac{A_3 g_{m1} R_L}{1 + A_3 g_{m2} R_L} V_{OS1} \underset{A_3 g_{m1} R_L \gg 1}{\cong} \frac{g_{m1}}{g_{m2}} V_{OS1} \tag{19}$$

During the *signal processing phase*, the K_1, K_3 and K_4 switches are turned *off* and K_2 is *on*.

During this phase transition, the voltage stored on the capacitor during the sampling phase is affected by the charge injection effects.

The AZT amplifier voltage gain, A_1, is:

$$A_1 = g_{m1}\, R_L, \tag{20}$$

where R_L is the load impedance.

Considering all these effects, the output voltage of the amplifier in this phase will become:

$$V_{out} = A_1 \left(V_{IN} + V_{OS} - \frac{A_2 A_3}{1 + A_2 A_3} V_{OS} \right) - A_2 \frac{q''_{inj} - q'_{inj}}{C_h}. \tag{21}$$

The input referred residual offset, $V_{os,rez}$, is defined as the output voltage corresponding to V_{in}=0 divided by the differential voltage gain.

$$V_{OS,rez} = \frac{V_o\,|_{V_{in}=0}}{A_1} = \frac{V_{OS1}}{A_2 A_3} - \frac{g_{m2}}{g_{m1}} \frac{q_{inj}}{C_h}. \tag{22}$$

The residual offset voltage has two components. The first component is given by the loop gain finite value (the input stage offset is not completely eliminated but only divided by the loop gain). The second component corresponds to the charge injection error.

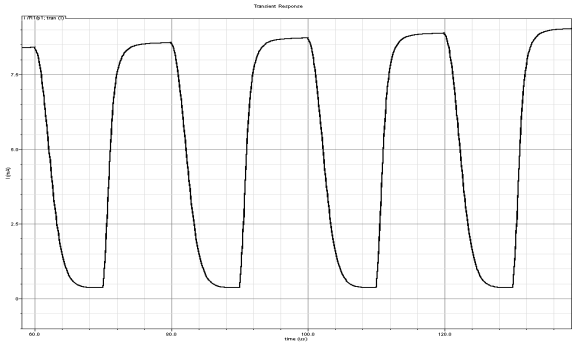

Fig. 6. Sense current without the S/H circuit.

7. Practical implementation

The autozero amplifier described above is used for controlling the sense current feedback loop. A standard comparator topology is used for comparing the sense voltage with the reference.

The autozero amplifier, A_1, compares the source voltages of the power and sense DMOS transistors and controls a feedback loop designed to keep the two source voltages equal. However, as discussed in the previous section, the amplifier is active only during the signal processing phase.

During the offset sampling phase, the amplifier output is brought to an internal reference value, independent of the input voltages. During this phase, the sense current control loop is broken.

To solve this problem, a sample and hold circuit was added to the A_1 amplifier output. This act as a current sample and hold circuit on the sense current as the A_1 output controls the sense transistor drain voltage through M_3 transistor.

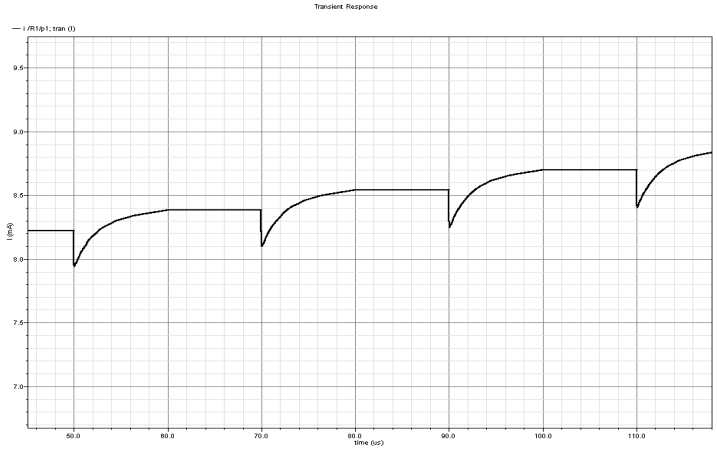

Fig. 7. Sense current with the S/H circuit.

Figure 6 shows the sense current behavior without the S/H circuit (autozero amplifier output is connected to M_3 gate). The sense current has the correct value during the signal processing phase, but jumps to an arbitrary value during the offset sampling phase. In Fig. 7 the S/H circuit was added. The sense current follows the output current (divided by K_{ILIS}) during the signal processing phase and remains constant during the offset sampling phase.

This approach introduces a delay in the current sensing process. If an over-current event occurs during the offset sampling phase, it will not be detected until the signal processing phase. However the over current signal is filtered against spikes, so the additional delay is not important.

8. Design flow

The target over current threshold is 1 A. Choosing a K_{ILIS} ratio of 100, results in a sense current threshold, I_{sense}, of 10 mA. A 5 V supply voltage is used. For testing the over current threshold, the load current is swept between 0 and 1 A in a 1 ms time interval, (see Fig. 8a). [5]

The A_1 autozero amplifier output and the sample and hold output signals are presented in Fig. 8b. The autozero output switches between the correct feedback signal (in signal processing phase) and the internal reference (in offset correction phase). The sample and hold circuit filters the autozero switching and provides the appropriate feedback signal on both phases.

Fig. 5c presents the A_2 comparator inputs: the sense voltage, obtained by applying the sense current on R_S resistor and the comparison reference. It can be seen that the sense voltage still has some spikes induced by the sample and hold process. The reference voltage should be inside A_2 common mode input voltage range, and should also be much larger than its offset voltage. To achieve this, we choose a 2.5 V reference.

When the sense voltage crosses the reference, the over current condition is detected, as shown in Fig. 5d. This happens at a load current of 1 A, as predicted by the equation (20).

$$I_{load} = K \frac{R_{ref}}{R_{sense}} I_{ref} = 100 \frac{2.5\,V}{250\,\Omega} = 1\,A. \tag{23}$$

The power transistor drain-source voltage drop at the transition point, $V_{DS,load}$, is given by the device on state resistance multiplied by the current threshold. In our case, $R_{DS,on} = 200$ mΩ resulting in a 200 mV drain-source voltage drop.

Taking this into account, we can evaluate the residual offset effect on the K_{ILIS} accuracy. Using equation (11), and consider a perfect power to sense transistor matching ($K_{load}/K_{sense} = 100$) we get a K_{ILIS} value of 100.05 so the residual offset error is about 0.05%.

This result should be compared with the case a standard A_1 amplifier topology is used. In this case, for a standard MOS process, the offset voltage is around 10 mV. This results in a K_{ILIS} value of 105.3, leading to a 5.3% error.

The A_1 autozero amplifier residual offset voltage, taking into account both the charge injection and base amplifier offset contributions, resulted below 100 μV.

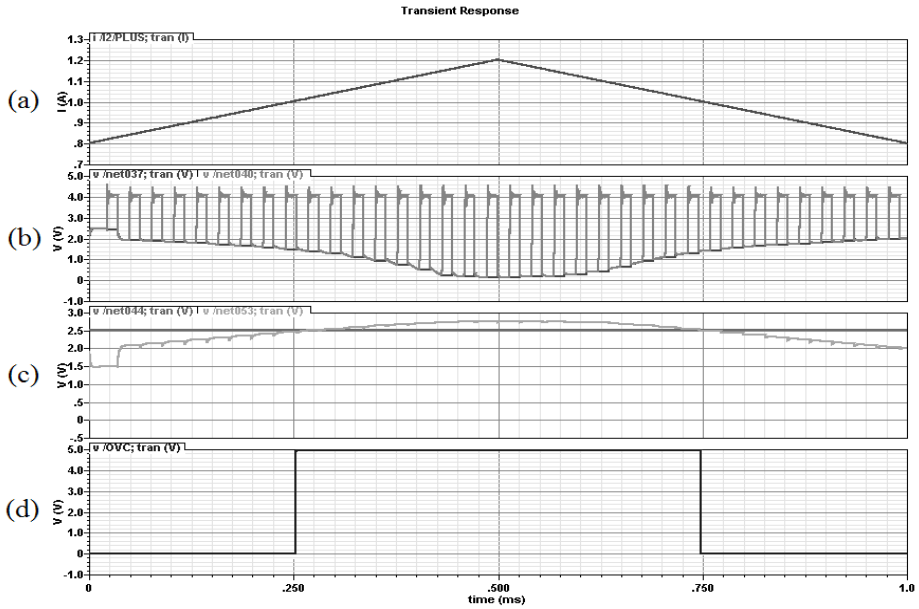

Fig. 8. The output response.

9. Conclusions

This paper presents a high precision over-current protective concept, implemented in a high side power switch. The load current is detected using a sense transistor, matched with the power switch. The same bias conditions for devices are provided by a feedback loop.

The current mirroring accuracy is strongly dependent on the main amplifier offset voltage, especially for low current threshold or low on state resistance, as the offset introduces a mismatch between main and sense transistors drain – source voltages.

For achieving good accuracy, the main amplifier offset voltage is reduced by implementing the autozero technique.

The autozero technique involves a two-phase functionality; one phase for sampling the offset and the other one for processing the signal.

The main amplifier can be connected in the feedback loop only during the signal processing phase, when it provides a valid output voltage. To this end, a sample and hold circuit controls the sense current while the main amplifier is in the offset sampling phase.

References

[1] Infineon Technologies AG, *Bringing theory into Practice: Fundamentals of Power semiconductors for Automotive applications*, September 2006, ISBN-13:978-0-9789866-0-5.

[2] LUCA A.-M., TRANCA I.-A., DANCHIV A., *High Precision over Current Detection for a High Side Switch*, CAS 2008, Sinaia, Romania, October 13–15, Vol. **2**, 2008.

[3] ENZ C. C., TEMES G. C., *Circuits Techniques for Reading the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling and Chopper Stabilization*, *Proceedings of the IEEE*, Vol. **84**, No. 11, Nov. 1996.

[4] DANCHIV A., BODEA M., DAN C., *Autozero Transconductance Amplifier Systematic Manual Design*, Sept. 2006.

[5] ALLEN P. E., HOLBERG D. R., *CMOS Analog Circuit Design*, Oxford University Press.