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Enhanced wide range tunable CMOS transconductor for signal processing

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Abstract.

An enhanced wide range current controlled CMOS transconductor is presented. The proposed circuit relies on the behavior of a current controlled current amplifier that uses an unbalanced current mirror. A fifth-order low pass filter based on the enhanced tunable transconductor is also presented as application.

Key-words: Transconductor, OTA, tunable trans-conductance, low noise, analog filter.

1. Introduction and preliminary results

The electrical control of the transconductance gain is mandatory for the component blocks used in the implementation of the $G_m - C$ adaptive signal processing filters. Given the limited resolution of the discrete control and due to the inherent non-ideal behavior of the switches, the continuous mode of control is often preferred to the discrete one, usually implemented by switching passive components like capacitors. The compensation of the passive components process variation requires a wide range, high-resolution control that can only be done by implementing a continuous or a mixed (continuous and discrete) type electrical control. This requirement makes the wide range electrically controlled transconductors crucial in $G_m - C$ adaptive filters design.

A large number of articles in the literature deal with the problem of transconductance adjusting and offer various solutions for this. In [1] a differential pair with variable degeneration resistance is used for the implementation of a continuously tunable transconductor. Source degeneration is also used in [2] by means of highly linear tunable active resistors. [3] presents a moderate range continuous tunable pseudo-differential CMOS transconductor. A digitally adjusted in coarse steps and a continuously adjusted in fine steps solution is proposed in [4], but the area cost is high due to the discrete tuning. Two balanced electronically programmable current mirrors operating in moderate inversion are used in the tunable transconductor that is proposed in [5] and a wide range tuning of G_m is possible using a $1 \div 140\,\mu\text{A}$ control current. In [6] a linear and tunable triode transconductor that employs a local negative feedback and obtains a

tuning range of about $\pm 35\,\%$ is presented. A gain squaring technique is used in the transconductor presented in [7] and a wide range G_m is achievable but with the cost of an equally wide range control bias current. A $\pm 50\,\%$ mirror gain range is achievable in a tunable transconductor that is proposed in [8] using a current mirror with triode operating transistors as degeneration, but the control is nonlinear. [9] presents an adjustable transconductor comprised of a simple differential stage with source resistive degeneration used to convert the input differential voltage to a differential current which is fed to a current-controlled current amplifier implemented with an unbalanced current mirror that exhibits a wide tunable gain.

Compared to the previous work [9], the present solution describes an improved transconductor whose operation is based on the behavior of an alternative unbalanced mirror architecture that allows a better linearity for the filters in which it is used. An extended nonlinearity analysis is done. Also a noise analysis is done following the methodology presented in [10]. As application for the presented current controlled transconductor, a fifth-order low-pass filter is proposed.

2. Operation principle

The basic principle is first explained using the simplified circuit shown in Figure 1. On the V_{GS} loop of the Figure 1, one can write in DC:

$$V_{GS2} = V_{GS1} + V_{TUNE} \tag{1}$$

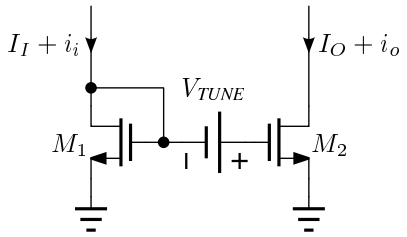

Fig. 1. Schematic of an unbalanced current mirror – simplified circuit

Using the square law for the MOS transistor and considering strong inversion for both devices, we obtain:

$$\sqrt{\frac{I_O}{I_I}} = 1 + \sqrt{\frac{K}{I_I}} V_{TUNE} \tag{2}$$

where I_O and I_I are the DC components of the output and input currents.

Related to the last relationship, we can note that the DC amplification becomes 1 if the tune voltage V_{TUNE} is 0. Also, if I_I is a bias current, $I_I = I_B$, the output current is going to be a $\left(1 + V_{TUNE}\sqrt{K/I_B}\right)^2$ amplified version of that bias current.

One can write for small signal components:

$$i_o = g_{m2} v_{gs2} \tag{3}$$

where $g_m = 2\sqrt{K I_M}$ is the transconductance of the transistor and:

$$v_{gs2} = v_{gs1} = \frac{i_i}{g_{m1}} \tag{4}$$

Using (2):

$$\frac{i_o}{i_i} = \frac{g_{m2}}{g_{m1}} = \sqrt{\frac{I_O}{I_I}} = 1 + \sqrt{\frac{K}{I_I}} V_{TUNE} \tag{5}$$

The last result shows that the proposed structure can be used as a voltage controlled current amplifier.

A practical way to implement the voltage source of the Figure 1 circuit is to use a resistor and a tune DC current, as Figure 2 shows.

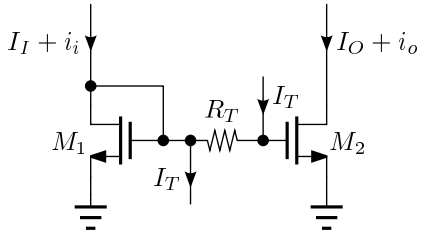

Fig. 2. Schematic of an unbalanced current mirror – circuit implementation

The DC relation between the currents of the structure from Figure 2 is:

$$\sqrt{\frac{I_O}{I_I}} = 1 + R\sqrt{\frac{K}{I_I}} I_T \tag{6}$$

The corresponding relationship between the small signal components:

$$\frac{i_o}{i_i} = \frac{g_{m2}}{g_{m1}} = \sqrt{\frac{I_O}{I_I}} \tag{7}$$

By combining the last two relationships and considering that the input DC component is a constant bias current, $I_I = I_B$:

$$a_i(I_T) = \frac{i_o}{i_i} = 1 + R\sqrt{\frac{K}{I_B}} I_T \tag{8}$$

The last result shows the current controlled current amplifier behavior of the proposed circuit. The current gain is higher as I_T is higher and I_B lower.

3. The proposed tunable transconductor

Using a source resistive degenerated differential pair, two cascoded instances of the previously presented unbalanced current mirror and two additional p-mos cascoded current mirrors, an enhanced tunable tranconductor is obtained as Figure 3 shows. Compared to the transconductor structure proposed in [9], giving the fact that in this circuit the tune resistor is no longer

connected in series to the master of the current mirror used as current amplifier, the dynamic range at the input of this transconductor is improved.

Considering the degenerative resistance large enough and $R_{S1} = R_{S2} = R_S$, the input differential pair currents are going to be:

$$\begin{cases} i_{I1} = I_B + \frac{v_{ID}}{2R_S} \\ i_{I2} = I_B - \frac{v_{ID}}{2R_S} \end{cases} \tag{9}$$

Using the results of the unbalanced current mirror analysis, relation (8), on the M_4-M_6-M_8 and M_3-M_5-M_7 structures:

$$\begin{cases} i_{o1} = a_i\left(I_T\right) i_{i1} = +a_i\left(I_T\right) \frac{v_{id}}{2R_S} \\ i_{o2} = a_i\left(I_T\right) i_{i2} = -a_i\left(I_T\right) \frac{v_{id}}{2R_S} \end{cases} \tag{10}$$

The differential output current can be expressed as:

$$i_{od} = \frac{i_{op} - i_{on}}{2} = i_{o1} - i_{o2} = a_i\left(I_T\right) \frac{v_{id}}{R_S} \tag{11}$$

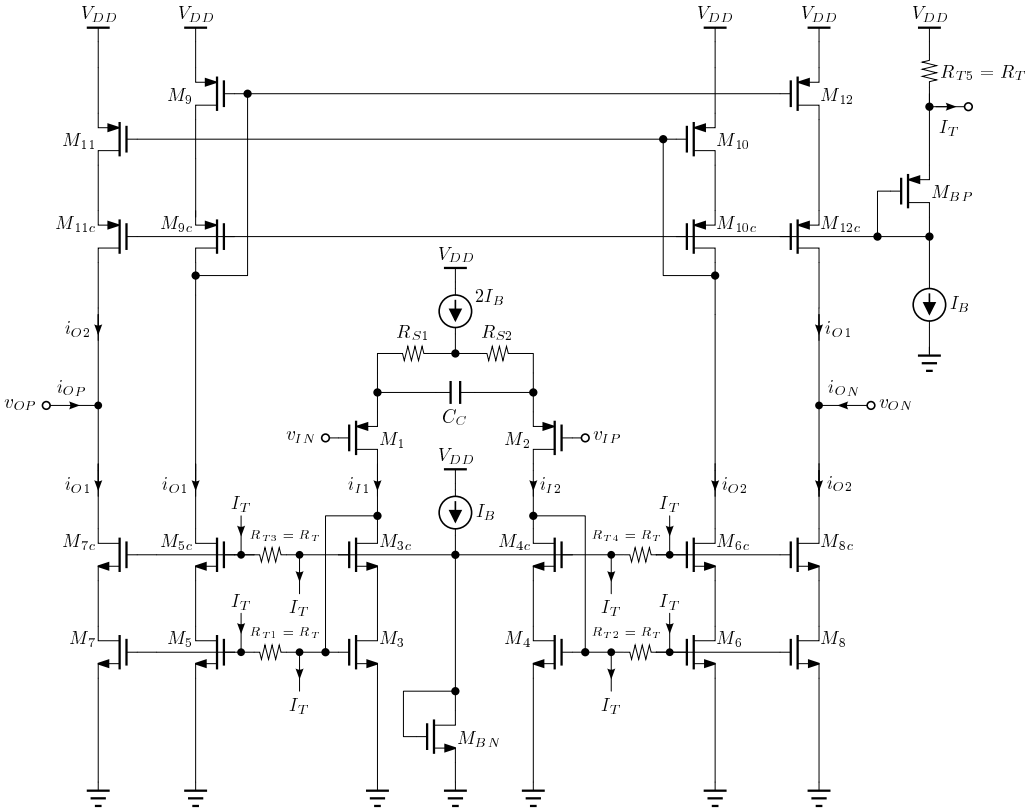

Fig. 3. Schematic of the proposed tunable transconductor

Consequently the transconductance can be written:

$$G_m = \frac{\partial i_{od}}{\partial v_{id}} = \frac{a_i(I_T)}{R_S} \tag{12}$$

Using (8):

$$G_m = \frac{1}{R_S}(1 + R_T\sqrt{\frac{K}{I_B}I_T}) \tag{13}$$

The last relationship shows that the transconductance of the proposed circuit is tunable by the I_T current.

4. Frequency analysis

The frequency analysis is done with the focus on the $G_m - C$ integrator as presented in Figure 4 simplified circuit, where C_C is the phase delay compensation capacitor, C_G is the total capacitance in the M_7 gate node and C_O is the output capacitance.

The transfer function expression is:

$$H(s) = \frac{V_O(s)}{V_I(s)} = \frac{A_0(1 + \frac{s}{z})}{(1 + \frac{s}{p_1})(1 + \frac{s}{p_2})(1 + \frac{s}{p_3})} \tag{14}$$

where:

$$\begin{array}{ll} z = \frac{1}{2C_C R_S} & p_1 = \frac{1}{C_O R_O} \\ p_2 = \frac{g_{m3}}{C_G(1+g_{m3}R_T)} & p_3 = \frac{1+g_{m1}R_S}{2C_C R_S} \end{array} \tag{15}$$

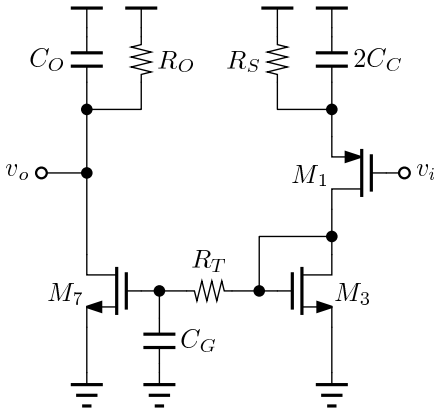

Fig. 4. Simplified circuit for frequency analysis of the $G_m - C$ integrator

5. Transconductor nonlinearity analysis

For the nonlinearity analysis of the transconductor we have used the square-law model for the MOS transistor and we have considered that the input stage (M_1, M_2, R_{S1} and R_{S2}) is linear due to the degeneration resistors, so relations (9) hold.

On the M_5, M_3, R_{T1} loop one can write:

$$v_{GS5} = v_{GS3} + R_T I_T \tag{16}$$

which can be written as:

$$K\left(v_{GS5} - V_{TH}\right)^2 = K\left(v_{GS3} - V_{TH}\right)^2 + \\ + 2K\left(v_{GS3} - V_{TH}\right) R_T I_T + K R_T^2 I_T^2 \tag{17}$$

that is equivalent to:

$$i_{O1} = i_{I1} + 2\sqrt{K} \cdot \sqrt{i_{I1}} \cdot R_T I_T + K R_T^2 I_T^2 \tag{18}$$

A similar result is obtained for i_{O2}:

$$i_{O2} = i_{I2} + 2\sqrt{K} \cdot \sqrt{i_{I2}} \cdot R_T I_T + K R_T^2 I_T^2 \tag{19}$$

The differential output current will be:

$$i_{OD} = \frac{i_{O1} - i_{O2}}{2} = \frac{i_{I1} - i_{I2}}{2} + \sqrt{K} \cdot R_T I_T \left(\sqrt{i_{I1}} - \sqrt{i_{I2}}\right) \tag{20}$$

Using (9):

$$i_{OD} = \frac{v_{ID}}{2R_S} + \sqrt{K} \cdot R_T I_T \left(\sqrt{i_{I1}} - \sqrt{i_{I2}}\right) \tag{21}$$

We expand $i_{OD}(v_{ID})$ in Taylor series up to the third term around $v_{ID} = 0$ in order to obtain an expression of the form:

$$i_{OD} = f\left(v_{ID}\right) = a_0 + a_1 v_{ID} + a_2 v_{ID}^2 + a_3 v_{ID}^3 \tag{22}$$

The first, second and third order derivatives of the (21):

$$\frac{\partial i_{OD}}{\partial v_{ID}} = \frac{1}{2R_S}\left[1 + \frac{\sqrt{k} R_T I_T}{2}\left(\frac{1}{\sqrt{i_{I1}}} + \frac{1}{\sqrt{i_{I2}}}\right)\right] \tag{23}$$

$$\frac{\partial^2 i_{OD}}{\partial v_{ID}^2} = \frac{\sqrt{k} R_T I_T}{16 R_S^2}\left(\frac{-1}{\sqrt{i_{I1}^3}} + \frac{1}{\sqrt{i_{I2}^3}}\right) \tag{24}$$

$$\frac{\partial^3 i_{OD}}{\partial v_{ID}^3} = \frac{3\sqrt{k} R_T I_T}{64 R_S^3}\left(\frac{1}{\sqrt{i_{I1}^5}} + \frac{1}{\sqrt{i_{I2}^5}}\right) \tag{25}$$

In order to write the Taylor series for $i_{OD}(v_{ID})$ up to the third power of v_{ID} we have to compute i_{OD}, $\frac{\partial i_{OD}}{\partial v_{ID}}$, $\frac{\partial^2 i_{OD}}{\partial v_{ID}^2}$ and $\frac{\partial^3 i_{OD}}{\partial v_{ID}^3}$ around $v_{ID} = 0$ when $i_{I1} = i_{I2} = I_B$:

$$a_0 = i_{OD}|_{v_{ID}=0} = 0 \tag{26}$$

$$a_1 = \left.\frac{\partial i_{OD}}{\partial v_{ID}}\right|_{v_{ID}=0} = \frac{1}{2R_S}\left(1+\sqrt{k}R_T\frac{I_T}{\sqrt{I_B}}\right) \tag{27}$$

$$a_2 = \left.\frac{\partial^2 i_{OD}}{\partial v_{ID}^2}\right|_{v_{ID}=0} = 0 \tag{28}$$

$$a_3 = \left.\frac{\partial^3 i_{OD}}{\partial v_{ID}^3}\right|_{v_{ID}=0} = \frac{3\sqrt{k}R_T}{32R_S^3}\frac{I_T}{\sqrt{I_B^5}} \tag{29}$$

Finally, we can write:

$$THD \approx \frac{1}{4}\left|\frac{a_3}{a_1}\right| V_{id}^2 = \frac{3\sqrt{k}R_T I_T}{64R_S^2 I_B^2\left(\sqrt{I_B}+\sqrt{k}R_T I_T\right)}V_{id}^2 \approx \frac{3}{64R_S^2 I_B^2}V_{id}^2 \tag{30}$$

6. Transconductor noise analysis

The noise analysis is carried out on the Figure 5 simplified differential half-circuit of the transconductor. The noise sources are considered uncorrelated. The i_{noh} noise current source is the noise due to the other half of the differential half-circuit.

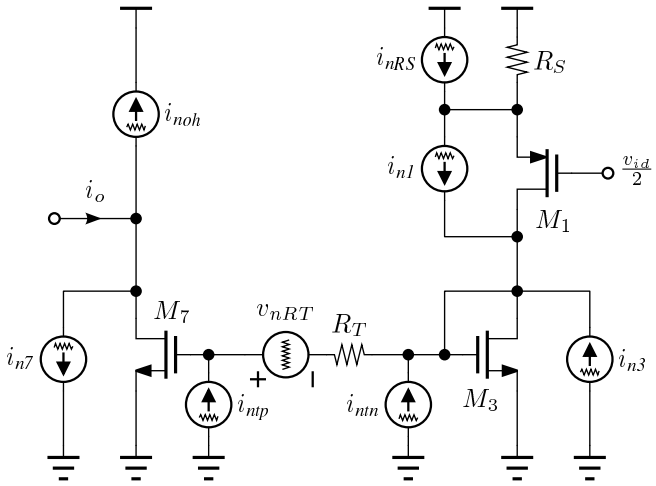

Fig. 5. Differential half-circuit of the transconductor with added noise sources

The resulting noise in the output can be written as:

$$i_{no} = i_{noh} + i_{n7} + g_{m7}v_{nRT} + (R_T + 1/g_{m3})\,g_{m7}i_{ntp} + \\ + \frac{g_{m7}}{g_{m3}}\left[i_{ntn} + i_{n3} + \left(\frac{g_{m1}R_S}{1+g_{m1}R_S}i_{nRS} + \frac{1}{1+g_{m1}R_S}i_{n1}\right)\right] \tag{31}$$

Thus the power spectral density (PSD) of the output noise current results as:

$$\overline{i_{no}^2} = \overline{i_{noh}^2} + \overline{i_{n7}^2} + g_{m7}^2 v_{nRT}^2 + (1 + g_{m3} R_T)^2 \left(\frac{g_{m7}}{g_{m3}}\right)^2 \overline{i_{ntp}^2} + \\ + \left(\frac{g_{m7}}{g_{m3}}\right)^2 \left[\overline{i_{ntn}^2} + \overline{i_{n3}^2} + \left(\frac{g_{m1} R_S}{1 + g_{m1} R_S}\right)^2 \overline{i_{nRS}^2} + \left(\frac{1}{1 + g_{m1} R_S}\right)^2 \overline{i_{n1}^2}\right] \quad (32)$$

Due to the fact that the other half of the differential half-circuit has identical noise characteristics, we can substitute $\overline{i_{noh}^2}$ with the rest of the above expression, thus the output noise current PSD becomes

$$\overline{i_{no}^2} = 2\Bigg\{\overline{i_{n7}^2} + g_{m7}^2 v_{nRT}^2 + (1 + g_{m3} R_T)^2 \left(\frac{g_{m7}}{g_{m3}}\right)^2 \overline{i_{ntp}^2} + \\ + \left(\frac{g_{m7}}{g_{m3}}\right)^2 \left[\overline{i_{ntn}^2} + \overline{i_{n3}^2} + \left(\frac{g_{m1} R_S}{1 + g_{m1} R_S}\right)^2 \overline{i_{nRS}^2} + \left(\frac{1}{1 + g_{m1} R_S}\right)^2 \overline{i_{n1}^2}\right]\Bigg\} \quad (33)$$

In order to refer the output noise to the input of the transconductor one must divide the output noise current power spectral density by the square of the overall transconductance $G_m = \frac{g_{m1}}{1+g_{m1} R_S} \frac{g_{m7}}{g_{m3}}$. Therefore the input noise voltage PSD can be written as:

$$\overline{v_{ni}^2} = 2 \left(\frac{1 + g_{m1} R_S}{g_{m1}} \frac{g_{m3}}{g_{m7}}\right)^2 \overline{i_{n7}^2} + \left(\frac{1 + g_{m1} R_S}{g_{m1}}\right)^2 g_{m7}^2 v_{nRT}^2 + \\ + 2 \left(\frac{1 + g_{m1} R_S}{g_{m1}}\right)^2 (1 + g_{m3} R_T)^2 \overline{i_{ntp}^2} + 2 \left(\frac{1 + g_{m1} R_S}{g_{m1}}\right)^2 \cdot \\ \cdot \left(\overline{i_{ntn}^2} + \overline{i_{n3}^2}\right) + 2 R_S^2 \overline{i_{nRS}^2} + 2 \left(\frac{1}{g_{m1}}\right)^2 \overline{i_{n1}^2} \quad (34)$$

Considering only thermal noise for the transistors the expression of the input noise voltage PSD becomes

$$\overline{v_{ni}^2} = 2 \cdot 4kT\gamma \Bigg\{ \left(\frac{1 + g_{m1} R_S}{g_{m1}}\right)^2 \left[\left(\frac{g_{m3}}{g_{m7}}\right)^2 g_{m7} + (1 + g_{m3} R_T)^2 g_{mtp} + \\ + g_{m3}^2 \frac{R_T}{\gamma} + g_{mtn} + g_{m3}\right] + \frac{R_S}{\gamma} + \frac{1}{g_{m1}} \Bigg\} \quad (35)$$

In order to simplify this expression, we will consider the numerical values for the small signal parameters. For the nominal cut-off frequency of 2 MHz, for which the tuning current has the value of $12.5\,\mu$A, the small signal parameters of the devices of the transconductor have the following approximate values:

- $R_T = 20\,\mathrm{k\Omega}$, $R_S = 100\,\mathrm{k\Omega}$,
- $g_{m1} = 20\,\mu\mathrm{S}$, $g_{m3} = 25\,\mu\mathrm{S}$, $g_{m7} = 400\,\mu\mathrm{S}$,
- $g_{mtp} = 130\,\mu\mathrm{S}$, $g_{mtn} = 220\,\mu\mathrm{S}$.

With these values we can write $g_{m3}R_T = 1/2$, $g_{m1}R_S = 2$, $g_{m3}/g_{m7} = 1/16$. It can be seen that the terms $(g_{m3}/g_{m7})^2 g_{m7}$, $g_{m3}^2 \frac{R_T}{\gamma}$ and g_{m3} are negligible with regard to the other terms in the sum, and the expression can be written:

$$\overline{v_{ni}^2} = \overline{v_{nGm}^2} = 2 \cdot 4kT\gamma \left\{ \left(\frac{1 + g_{m1}R_S}{g_{m1}} \right)^2 \left[(1 + g_{m3}R_T)^2 g_{mtp} + g_{mtn} \right] + \right.$$
$$\left. + \frac{R_S}{\gamma} + \frac{1}{g_{m1}} \right\} \quad (36)$$

Considering $\gamma = 2/3$ (for long channel transistors) the input noise voltage power spectral density has the value

$$\overline{v_{ni}^2} = \overline{v_{nGm}^2} \approx 260\,\mathrm{fV^2\,Hz^{-1}} \quad (37)$$

The theoretical analysis reveals the fact that the input referred noise can be further lowered by decreasing the transconductance of the tuning current sources transistors.

7. Implementation of a 5th order $G_m - C$ low pass filter

A 5th order $G_m - C$ low-pass filter has been designed as an application for the proposed tunable transconductor, with a nominal cut-off frequency of $f_c = 2\,\mathrm{MHz}$. It has been implemented as a cascade of first and second order sections, as illustrated in Figure 6.

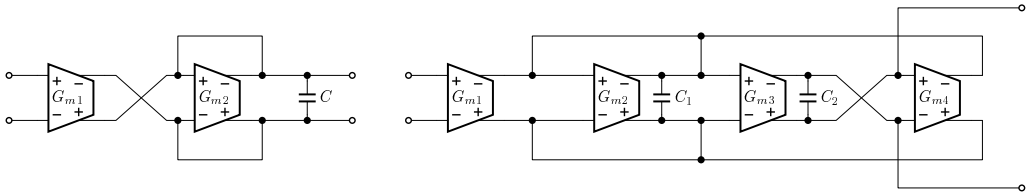

Fig. 6. First order (left) and second order (right) low pass sections used in the filter

The gain, cut-off frequency and Q factor of each biquad can be written as:

$$a_0 = \frac{G_{m1}}{G_{m4}} \quad (38)$$

$$f_c = \frac{\omega_c}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{G_{m3}G_{m4}}{C_1C_2}} \quad (39)$$

$$Q = \sqrt{\frac{C_1}{C_2}\frac{G_{m3}G_{m4}}{G_{m2}^2}} \quad (40)$$

The parameters of each filter section are given by the Table 1.

Table 1. Filter sections parameters

Filter section	G_m(at I_T=12.5 µA)	C_1	C_2	Q	f_c
1	91.96 µS	7.31 pF	–	–	2 MHz
2	91.96 µS	11.82 pF	4.51 pF	1.62	2 MHz
3	91.96 µS	4.51 pF	11.82 pF	0.62	2 MHz

The resulted 5th order low pass filter is presented in Figure 7. The elements G_{m1}, G_{m2} and C_1 implement the first order low pass $G_m - C$ section of the filter. The elements G_{m3}, G_{m4}, G_{m5}, G_{m6}, C_2 and C_3 implement the first second order low pass $G_m - C$ section of the filter. The elements G_{m7}, G_{m8}, G_{m9}, G_{m10}, C_4 and C_5 implement the last second order low pass $G_m - C$ section of the filter. The second and third sections of the filter have different quality factors and our analysis shown the advantages of cascading placement from the noise and non-linearity point of view: the high Q biquad should be used as the second section and the low Q one as the third section of the filter.

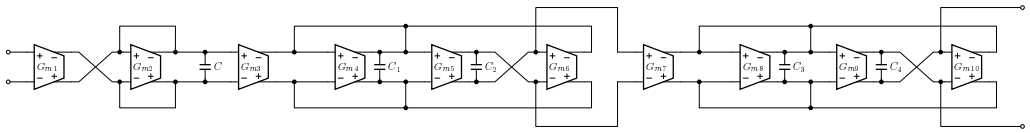

Fig. 7. 5th order $G_m - C$ low pass filter

8. Noise analysis of the filter sections

In order to determine the equivalent input referred noise of the filter, the effect of all the contributions due to individual transconductors of each section in the output is determined and referred back to the input of the filter. The equivalent input noise voltage sources of the transconductors are represented in the differential half-circuit of each section – Figure 8 and Figure 9 – and the transfer functions from each noise source to the output has been determined [10].

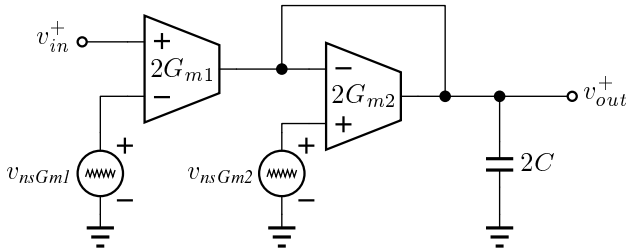

Fig. 8. Single pole filter section differential half-circuit with noise

The transfer functions from v_{nsGm1} and v_{nsGm2} to v_{out}^{+} are, respectively,

$$H_{nsGm1}(s) = \frac{\frac{G_{m1}}{G_{m2}}\frac{G_{m2}}{C}}{s + \frac{G_{m2}}{C}} \tag{41}$$

$$H_{nsGm2}(s) = \frac{\frac{G_{m2}}{C}}{s + \frac{G_{m2}}{C}} \tag{42}$$

Therefore, the equivalent input referred voltage noise due to v_{nsGm1} and v_{nsGm2}, can be expressed as:

$$\overline{v_{insGm1}^2} = \left|\frac{H_{nsGm1}(j\omega)}{H_S(j\omega)}\right|^2 \overline{v_{nsGm1}^2} = \overline{v_{nsGm1}^2} \tag{43}$$

$$\overline{v_{insGm2}^2} = \left|\frac{H_{nsgm2}(j\omega)}{H_S(j\omega)}\right|^2 \overline{v_{nsGm2}^2} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \overline{v_{nsGm2}^2} \tag{44}$$

The total input referred noise becomes:

$$\overline{v_{ins}^2} = \overline{v_{insGm1}^2} + \overline{v_{insGm2}^2} = \overline{v_{nsGm1}^2} + \left(\frac{G_{m2}}{G_{m1}}\right)^2 \overline{v_{nsGm2}^2} \tag{45}$$

With $G_{m1} = G_{m2}$ and $\overline{v_{nsGm1}^2} = \overline{v_{nsGm2}^2} = \overline{v_{nGm}^2}$ the expression is written as:

$$\overline{v_{ins}^2} = 2\overline{v_{nGm}^2} \tag{46}$$

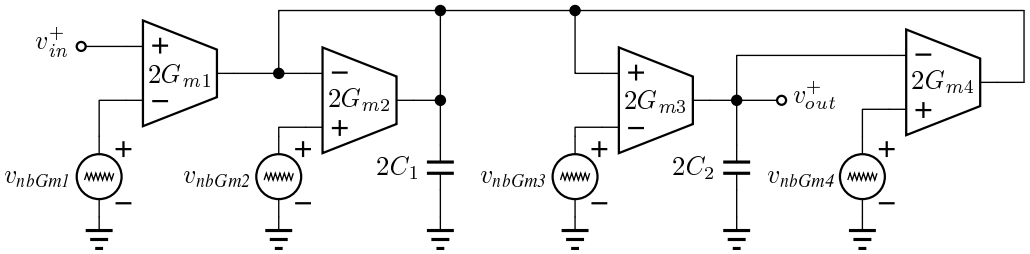

Fig. 9. Biquad filter section differential half-circuit with noise

The transfer functions from v_{nbGm1}, v_{nbGm2}, v_{nbGm3} and v_{nbGm4} to v_{out}^{+} are, respectively,

$$H_{nbGm1}(s) = \frac{\frac{-G_{m1}}{G_{m4}}\frac{G_{m3}G_{m4}}{C_1C_2}}{s^2 + \frac{G_{m2}}{C_1}s + \frac{G_{m3}G_{m4}}{C_1C_2}} \tag{47}$$

$$H_{nbGm2}(s) = \frac{\frac{G_{m2}}{G_{m4}}\frac{G_{m3}G_{m4}}{C_1C_2}}{s^2 + \frac{G_{m2}}{C_1}s + \frac{G_{m3}G_{m4}}{C_1C_2}} \tag{48}$$

$$H_{nbGm3}(s) = \frac{-\frac{G_{m3}}{C_2}s + \frac{G_{m2}}{G_{m4}}\frac{G_{m3}G_{m4}}{C_1C_2}}{s^2 + \frac{G_{m2}}{C_1}s + \frac{G_{m3}G_{m4}}{C_1C_2}} \tag{49}$$

$$H_{nbGm4}(s) = \frac{\frac{G_{m3}G_{m4}}{C_1C_2}}{s^2 + \frac{G_{m2}}{C_1}s + \frac{G_{m3}G_{m4}}{C_1C_2}} \tag{50}$$

Therefore, the equivalent input referred voltage noise due to v_{nbGm1}, v_{nbGm2}, v_{nbGm3} and v_{nbGm4}, can be expressed as [10]:

$$\overline{v_{inbGm1}^2} = \left|\frac{H_{nbGm1}(j\omega)}{H_B(j\omega)}\right|^2 \overline{v_{nbGm1}^2} = \overline{v_{inbGm1}^2} \tag{51}$$

$$\overline{v_{inbGm2}^2} = \left|\frac{H_{nbGm2}(j\omega)}{H_B(j\omega)}\right|^2 \overline{v_{nbGm2}^2} = \left(\frac{G_{m2}}{G_{m1}}\right)^2 \overline{v_{nbGm2}^2} \tag{52}$$

$$\overline{v_{inbGm3}^2} = \left|\frac{H_{nbGm3}(j\omega)}{H_B(j\omega)}\right|^2 \overline{v_{nbGm3}^2} = \left[\left(\frac{G_{m2}}{G_{m1}}\right)^2 + \left(\frac{\omega C_1}{G_{m1}}\right)^2\right] \overline{v_{nbGm3}^2} \tag{53}$$

$$\overline{v_{inbGm4}^2} = \left|\frac{H_{nbGm4}(j\omega)}{H_B(j\omega)}\right|^2 \overline{v_{nbGm4}^2} = \left(\frac{G_{m4}}{G_{m1}}\right)^2 \overline{v_{nbGm4}^2} \tag{54}$$

The total input referred noise becomes:

$$\overline{v_{inb}^2} = \overline{v_{inbGm1}^2} + \overline{v_{inbGm2}^2} + \overline{v_{inbGm3}^2} + \overline{v_{inbGm4}^2} = \overline{v_{nbGm1}^2} + \left(\frac{G_{m2}}{G_{m1}}\right)^2 \overline{v_{nbGm2}^2} + \\ + \left[\left(\frac{G_{m2}}{G_{m1}}\right)^2 + \left(\frac{\omega C_1}{G_{m1}}\right)^2\right] \overline{v_{nbGm3}^2} + \left(\frac{G_{m4}}{G_{m1}}\right)^2 \overline{v_{nbGm4}^2} \tag{55}$$

With $G_{m1} = G_{m2} = G_{m3} = G_{m4}$ and $\overline{v_{nbGm1}^2} = \overline{v_{nbGm2}^2} = \overline{v_{nbGm3}^2} = \overline{v_{nbGm4}^2} = \overline{v_{nGm}^2}$ the expression is written as:

$$\overline{v_{inb}^2} = \left[4 + \left(\frac{\omega C_1}{G_{m1}}\right)^2\right] \overline{v_{nGm}^2} = \left[4 + \left(\frac{\omega}{\omega_c}\right)^2 Q^2\right] \overline{v_{nGm}^2} \tag{56}$$

In the band of the filter, for $\omega \ll \omega_c$, the total input referred noise is the sum of the input referred noise of each section (because here the gain of each section is 1). Therefore:

$$\overline{v_{nifilter}^2} = (2 + 4 + 4)\,\overline{v_{nGm}^2} = 10\overline{v_{nGm}^2} \tag{57}$$

9. Simulation results

The proposed circuit was simulated using the models of an AMS $180\,\mathrm{nm}$ CMOS process. The tranconductor DC transfer characteristics, the frequency response, the G_m versus the tuning current and the THD of the output current are illustrated in Figure 10, Figure 11, Figure 12 and Figure 13.

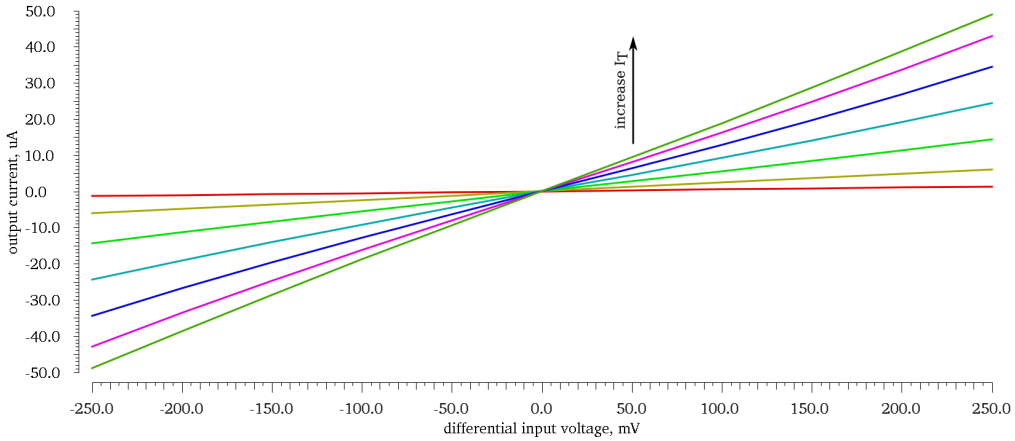

Fig. 10. Transconductor transfer characteristics, for different I_T values in the range $0\ldots25\,\mu\mathrm{A}$

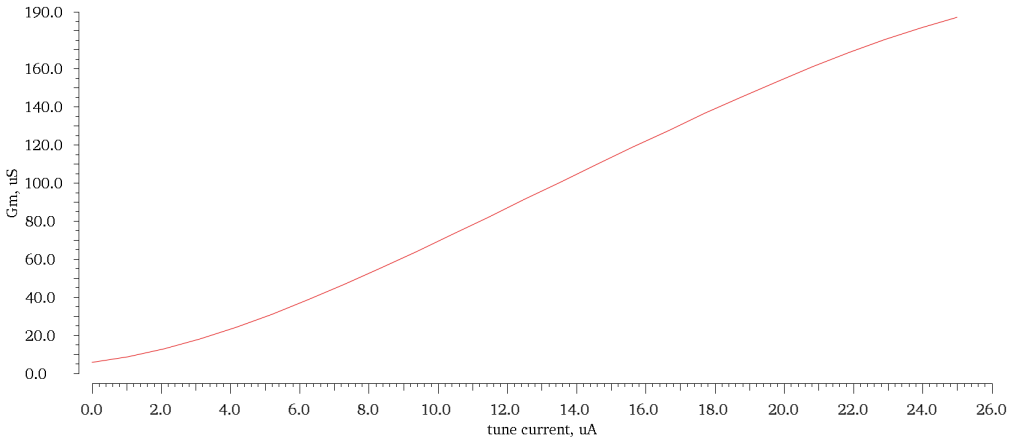

Fig. 11. G_m tuning range($92\,\mu\mathrm{S}\pm90\,\%$)

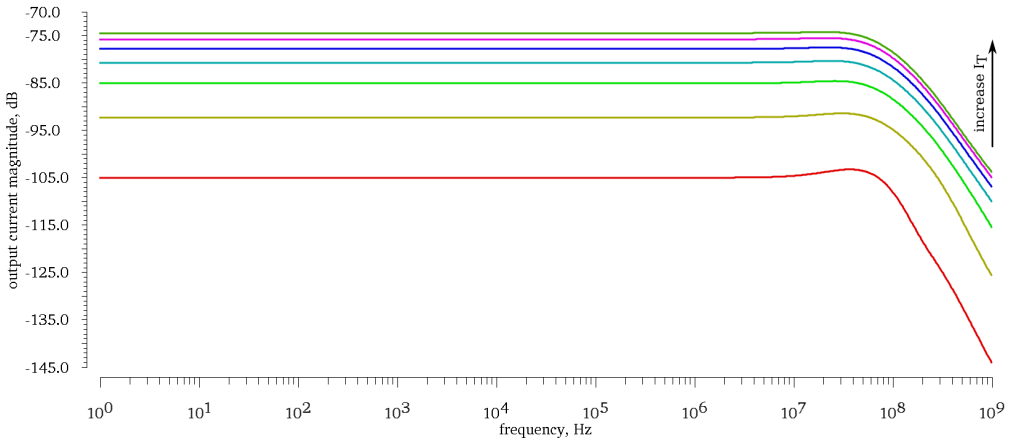

Fig. 12. Frequency response of the transconductor, for different I_T values in the range $0...25\,\mu A$

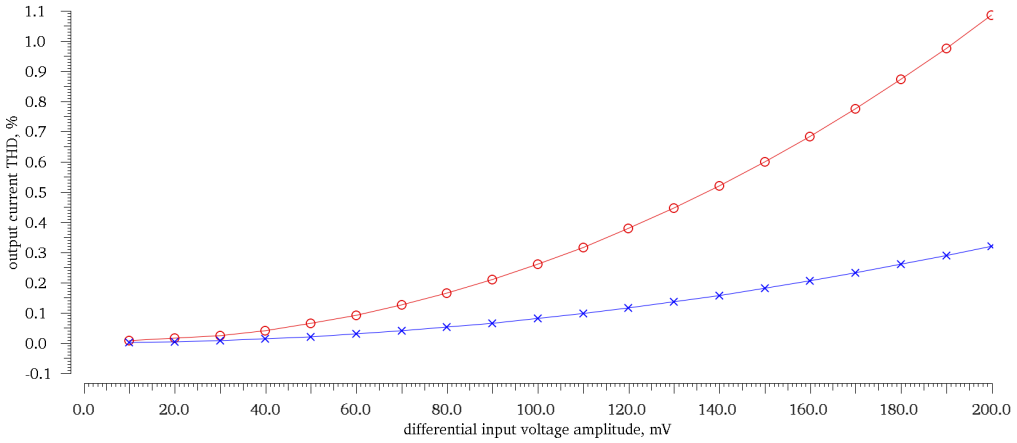

Fig. 13. THD at the output of the transconductor, simulation result (○) and theoretical calculus (x) for $I_T = 12.5\,\mu A$

The observable differences between the simulated and the theoretical characteristic of THD are justified by the quadratic model considered for the transistor and by the fact that the input source resistive degenerated differential input stage was considered linear.

The transconductor noise analysis simulation results gives a value of about $450\,fV^2\,Hz^{-1}$ in the region after the $1/f$ corner (flicker noise corner frequency, which is about $400\,kHz$), as shown in Figure 14. The obtained value for the input referred noise voltage power spectral density is comparable to the one obtained from the analysis, and it is higher because the theoretical analysis has been carried out on a simplified schematic, neglecting several less important noise contributors. The input referred noise voltage rises at high frequencies due to finite output noise current and the decrease in transconductance (due to high frequency poles).

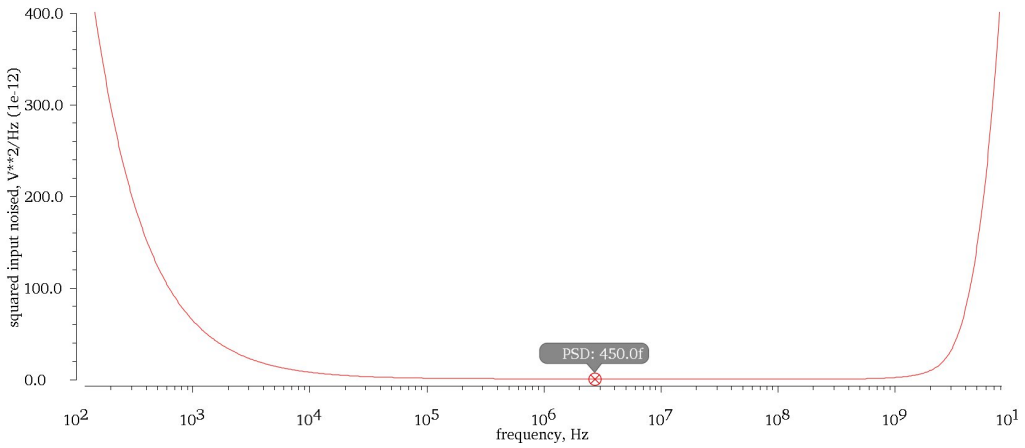

Fig. 14. Transconductor input referred noise voltage PSD

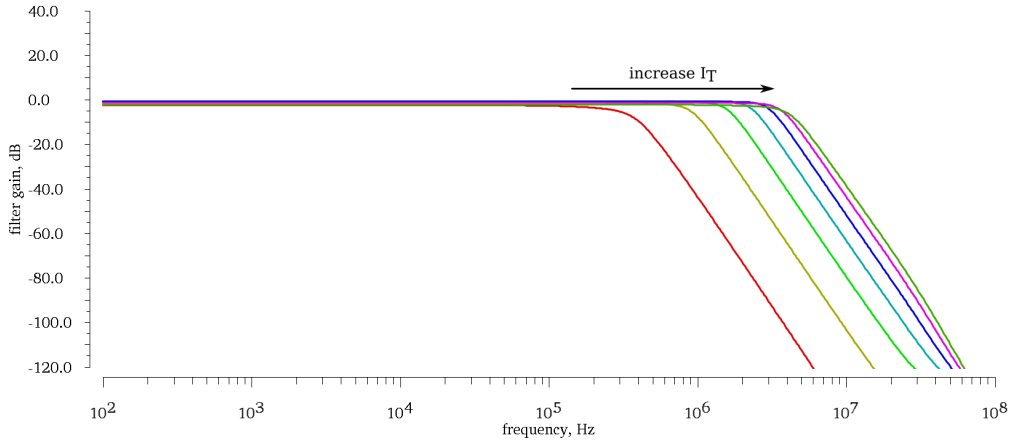

Fig. 15. Gain characteristics of the implemented filter, for different I_T values in the range $0...25\,\mu A$

The gain characteristic, the cutoff frequency versus the tune current and the THD of the filter output voltage are ploted in Figure 15, Figure 16 and Figure 17.

The equivalent squared input noise of the proposed filter is plotted in 18:

It can be observed that past the $1/f$ corner the squared input noise is about $6\,pV^2\,Hz^{-1}$, value which agrees to the theoretical analysis presented before. This value is about 10 times larger than the input squared noise of a transconductor instance.

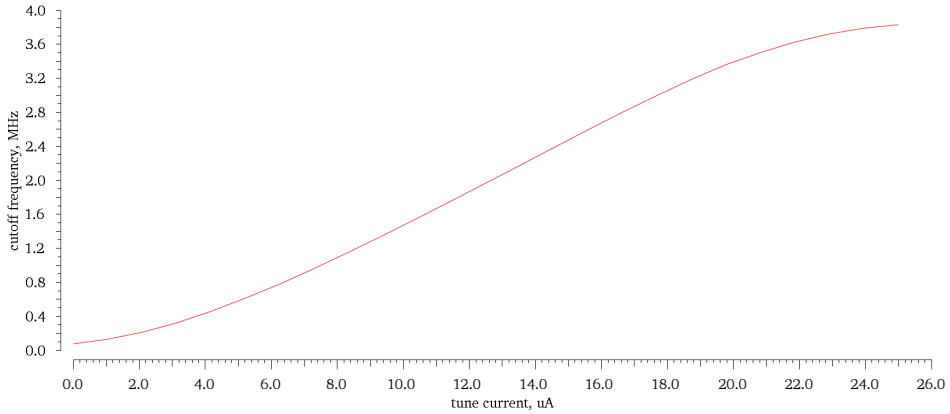

Fig. 16. Cut-off frequency tuning range: 2 MHz+/-90%

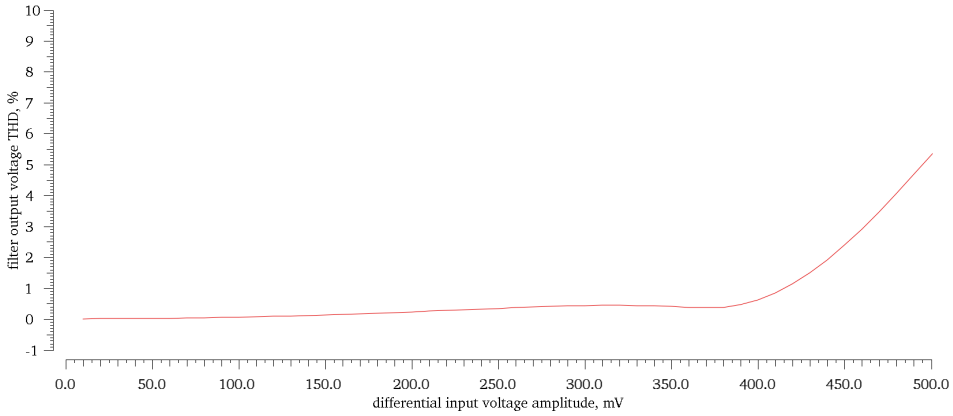

Fig. 17. Filter output THD

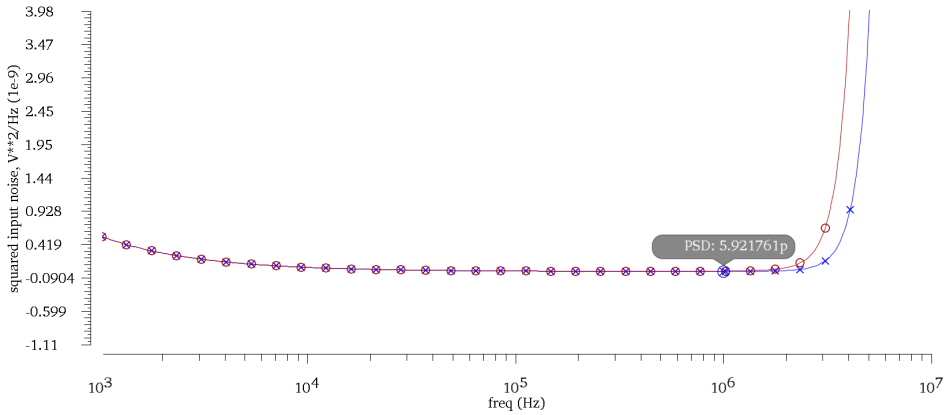

Fig. 18. Filter squared input referred noise, low Q — high Q cascade (○) and high Q -– low Q cascade (x)

Table 2. Compared performances of transconductor tunability

Measured performance	**[5]**	**[6]**	**[7]**	**This work**
G_m tuning range	$1\,\mu\text{S} \div 90\,\mu\text{S}$	$20\,\mu\text{S} \div 31.5\,\mu\text{S}$	$100\,\text{nS} \div 400\,\mu\text{S}$	$5\,\mu\text{S} \div 175\,\mu\text{S}$
Control range	$1\,\mu\text{A} \div 140\,\mu\text{A}$	$4.5\,\mu\text{A} \div 6.75\,\mu\text{A}$	$1\,\text{nA} \div 600\,\mu\text{A}$	$1\,\mu\text{A} \div 25\,\mu\text{A}$
$x = \frac{G_{m\,MAX}}{G_{m\,MIN}}$	90	1.6	4000	35
$y = \frac{I_{TUNE\,MAX}}{I_{TUNE\,MIN}}$	140	1.5	600×10^3	25
$\frac{x}{y}$	0.64	1.1	6.7×10^{-3}	1.4

10. Conclusions

The versatility of the unbalanced current mirror used as gain stage was presented in [9], allowing the design of a wide range tunnable transconductor. In this paper is proposed an alternative architecture of unbalanced current mirror which allows to obtain a better linearity of the $G_m - C$ filters that use it. The proposed G_m tune range is $92\,\mu\text{S} \pm 90\,\%$. Compared to works in [5–7], as shown in Table 2, the implemented transconductor exhibits a higher tuning range versus control range coefficient. As an application a fifth order low-pass $G_m - C$ filter was presented. Its cutoff frequency can be tuned in a $\pm 90\,\%$ range by varying the G_m tune current. The importance of the section order in the filter has been investigated with regard to the noise and nonlinearities. Simulations results show that the optimal configuration is the single pole – high Q -– low Q cascade. Theoretical analysis of noise for the transconductor instance and filter stages has been carried out and the obtained expressions show good agreement with the simulation results. The analysis shows that the noise performance can be further improved by scaling the I_T current sources transistors. Laboratory validation of simulation results is planned after the Q4 2018 manufacturing.

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