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Digitally controlled oscillator for all-digital frequency locked loops

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Abstract. A digitally controlled oscillator is presented as a suitable solution for all-digital frequency lock loops. The system consists of a bias circuit, current-voltage converters and a current controlled oscillator, which is implemented using log-domain circuits. In this way, the oscillation frequency can be tuned using the bias currents. The bias circuit consists of a binary decoder and a current division network. The role of the decoder is to control the output current values of the division network via a 10-bit digital control word. Thus, it was possible to obtain 1024 distinct bias current values which yielded 1024 frequency values. The current-voltage converter transforms the output current into a voltage necessary for the next stage. All circuits were implemented using Virtuoso Analog Design Environment from Cadence using a 180nm CMOS technology. The MOS transistors for the log-domain blocks are working in sub-threshold region. Spectre simulations were performed to demonstrate de functionality of the proposed circuit.

Key-words: DCO, ADFLL, ELIN, sub-threshold, log-domain.

1. Introduction

Frequency synthesizers are key circuits in many electronic systems, as they are employed for clock generation in digital circuits, clock and data recovery in serial communications, and carrier frequency generation in wireless communications. With the development of the aforementioned systems, the specifications for the frequency synthesizers are becoming bold, besides of the traditional performance metrics, the jitter and phase noise, new metrics, such as power consumption, lock time and wide frequency range are emerging. The general approach to frequency synthesis is to multiply the frequency of a reference signal, generated by a device with precise frequency, i.e. quartz crystal oscillator. The implementation of such frequency multipliers led to the development of phase locked loops (PLLs) [1].

Traditionally, PLLs are considered analog circuits, thus inherently are susceptible to noise and manufacturing process variations. Moreover, the analog circuit design flow is not adequate

for design reuse, because certain analog blocks must be redesigned when moving from one technology to another. To overcome this problem the "digitization" of PLLs took place, thus giving birth to the concept of all-digital phase locked loops (ADPLL) [2]. Lately, great interest surrounds the ADPLLs, because the digital nature of the loops promises robustness against process variations, less susceptibility to noise, fast locking control algorithms, shorter time-to-market, better design reuse. Still, ADPLLs contain a key component, a digitally controlled oscillator (DCO), which is unsuitable for digital implementation [3], current research efforts are focused on lowering power dissipation, occupied chip area, supply voltage while improving resolution and frequency range. A straightforward implementation of a DCO can be achieved by combining a voltage controlled oscillator (VCO) and a digital to analog converter (DAC). The DAC takes a binary control word and translates it into a voltage, which in turn drives the VCO to generate the oscillation frequency.

There are two main VCO implementations presented in the literature, one based on LC-tank [4–6] and the other based on the ring topology [7, 8]. LC VCO's are mostly implemented using passive inductors [4] leading to a poor quality factor at high frequencies. Another drawback is the large area occupied in silicon. The frequency tuning is achieved by switching on and off capacitance banks. The ring topology is mostly employed due to the small area and low power consumption. The typical implementation of a ring oscillator implies the use of current starved inverter stages, with variable propagation time with respect to the control voltage [5], but there are trials to achieve frequency tuning by switching the driving strength of the inverter, or switching the load capacitance [6]. In both cases the control voltage from the DAC is used for fine tuning the frequency.

Clearly, the future trend in frequency synthesis is the development of a fully synthesizable ADPLL in a digital design flow based on hardware description languages (HDL). Besides the ADPLL structure, possible candidates for frequency synthesis are the all-digital delay locked loop (ADDLL) and the all-digital frequency locked loop (ADFLL). None of the loops can miss a DCO, as a component. Regardless which architecture is used, a common cell, is an inverter with variable propagation time. In the ADDLL, a delay line - made from cascaded inverters - and an edge combiner is used to generate the oscillation. In the ADPLL and ADFLL the VCO could be achieved with the use of a ring oscillator made of inverters.

The rest of the paper is organized as follows. In Section 2 is presented an overview off all-digital phase/delay/frequency locked loops emphasizing the role of the DCO. Section 3 presents the proposed DCO architecture and the practical transistor level realization of the building blocks followed in Section 4 by the simulation results. Finally in Section 5 the final conclusions are presented.

2. All-digital loop architectures

In the following section, an overview of the all-digital phase/delay/frequency locked loops are given, with the intention of modeling the use of digitally controllable oscillator. While the structure of phase and frequency locked loops allows the use of an LC tank based oscillator, the delay locked loop main component is a delay line that consists of cascaded inverters with variable propagation time. Such inverters are also the building blocks of the ring oscillators. Moreover, the digital nature of the inverter cells, makes the delay line or ring oscillator more suitable for digital implementation, than the LC tank based oscillators.

The ADPLL [7] structure is depicted in Figure 1. As, the DCO is in the focus of this paper, let us discuss first this component. There are many possible implementations of the DCO. One is

to use a voltage controlled ring oscillator and a digital-to-analog converter (this implementation is depicted in the figure). The output of the DCO is usually a high frequency signal, noted OSC in the figure. The phase of the OSC signal should be compared with a precise phase of the signal noted REF, then it is divided by a Frequency Divider (FD).

There is a wide range of FD implementation. The most common one consists of the stages: a prescaling stage (the prescaller is implemented with high frequency D type flip-flops (DFFs), such as dynamic DFFs or true singe-phase clock DFFs [8]) and a programmable divider with N, where N gives the desired frequency set by the user with a numeric input denoted frequency control word FCW. The prescaller circuit divides the frequency with a constant number M. As N and M are integers, the frequency of OSC signal can be only integer multiple of the REF frequency. These implementations are known as integer-N phase locked loops. To obtain a fractional ratio between the OSC and REF frequencies, a technique called dithering is employed. Dithering consists of switching the divisor of the prescaller between M and M+1 with a control algorithm (constant modulus or sigma delta modulation are used). The output of the FD is a signal, which carries the phase of the OSC signal.

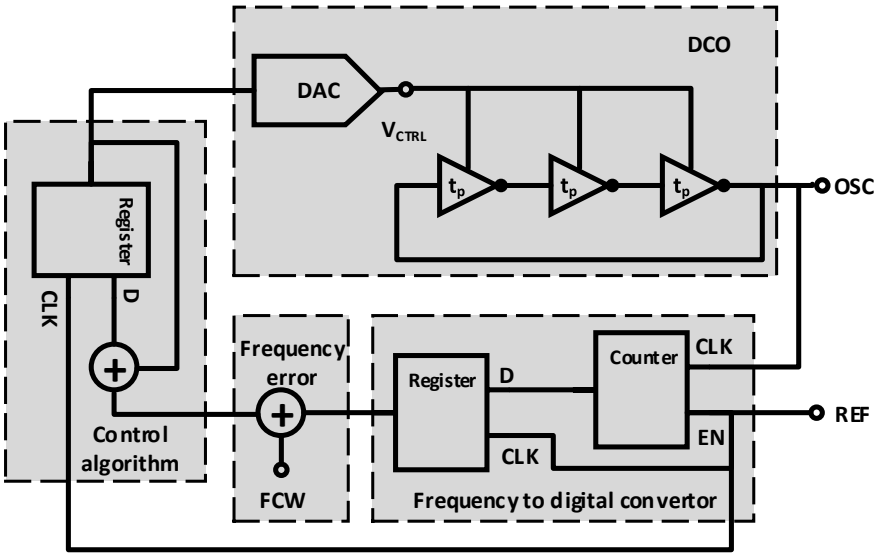

Fig. 1. The all-digital phase locked loop

The OSC and REF signal's phases are compared in the Phase Detector (PD). The traditional way of phase detection is with the use of a XOR gate. Modern solutions employ a time to digital converter (TDC) [9] to measure the time difference between the edges of the OSC and REF signal, thus obtaining the phase error. The phase error is then processed by a Control Algorithm. The typical control is a lowpass filter, called loop filter in the PLL terminology. The design procedure of the loop filter consists of: first an analog version of the PLL is achieved, next the "digitization" of the analog filter takes place, finally digital circuitry is used to implement the filter [10], [11]. While the loop filter in the analog PLL is easily implemented with a few components, its digital counterpart ends up in a power and area hungry FIR filter. Nevertheless,

the control algorithm does not need to be a loop filter. With the aid of a digital design flow, sophisticated algorithms could be easily implemented, algorithms that are not suited for analog implementations [12].

2.1. The all digital delay locked loop

The ADDLL [13] is depicted in Figure 2. In this structure, a delay line -made of N cascaded inverters- and an edge combiner circuit is used the multiply the input frequency. The desired frequency is controlled by the user with a numeric value noted frequency control word (FCW). With the aid of a multiplexer (MUX), the FCW will select one output from the delay line, thus configuring the effective length of the delay line (say 10 out of 100). The effective length of the delay line determines the frequency multiplication factor. The phase lock is achieved by comparing the phase of the MUX output with the phase of the REF signal. After a phase domain lock is achieved the same considerations apply for the Phase Detector and Control Algorithm blocks as for the ADPLL. The disadvantage of this structure is the integer frequency multiplication factor (the dithering technique is not suitable for this structure), the edge combiner (usually implemented with an XOR port array) and the MUX (made out of AND and OR gates), they are area and power-hungry circuits. The sole advantage is that no high frequency divider is required.

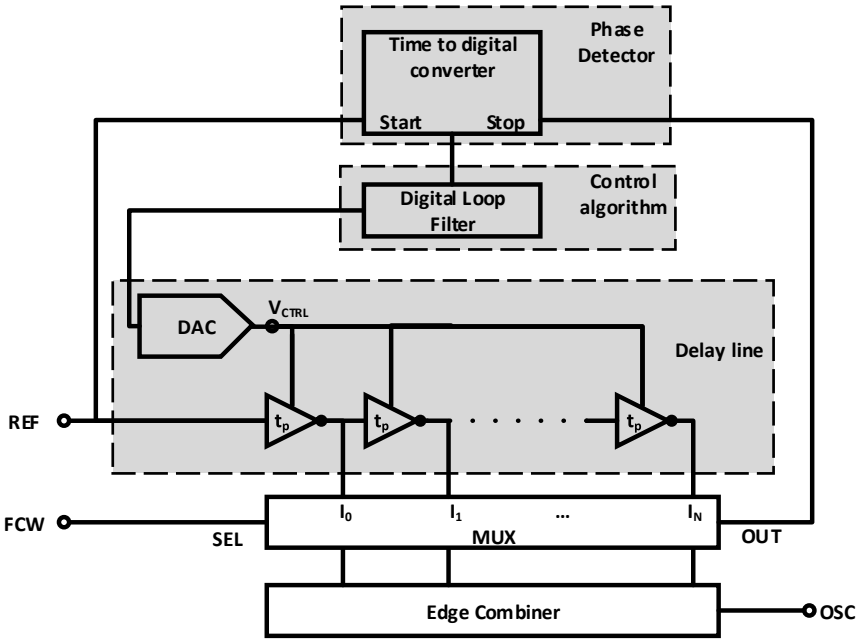

Fig. 2. The all-digital delay locked loop

2.2. The all digital frequency locked loop

The ADFLL architecture is depicted in Figure 3.

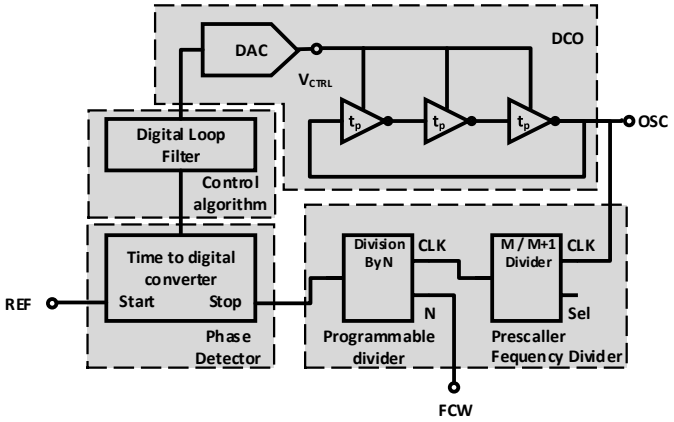

Fig. 3. The all-digital frequency locked loop

This solution comprises a DCO, a Frequency to digital converter (FDC) composed of a Counter and a Register, a Frequency error calculation stage, typically a subtraction circuit that computes the difference between frequency control word (FCW) and the current frequency given by the FDC and Control Algorithm. A possible solution for the control is a digital accumulator (integration in the discrete domain), which integrates the frequency error signal, thus computing the control word for the DCO [14], [15]. An advantage of the ADFLL is that the lock is achieved in the frequency domain, thus loop filter is replaced by a digital integrator, which is a significantly smaller circuit than a FIR filter. An important design parameter of the all-digital loops is the resolution of the DCO. Ref. [16] concluded that the higher the resolution of the DCO is, the better jitter performance is achieved, but the frequency lock is slower in the case of the ADFLL. But this observation is generally true for all-digital loops.

3. The proposed digitally controlled oscillator

The block schematics of the proposed digitally controlled oscillator is presented in Figure 4. It consists of a current controlled oscillator (CCO), a current-voltage converter and a bias circuit consisting of a current division network and a binary decoder. The CCO is implemented using Externally Linear Internally Nonlinear (ELIN), more precisely log-domain circuits. The frequency of the output current I_{out} of the log-domain implementation can be tuned using the bias currents I_B of the building blocks. The output voltage, V_{out}, of the DCO is obtained from the output current of the CCO using a current-voltage converter. The bias currents for the CCO cells are obtained using a current division network (CDN). The CDN is implemented using current division cells (CDC), the number of CDCs are equal to the number of desired bias current values. It is possible to obtain 1024 distinct bias current values using a 10 bit control word. The control word is applied to a binary decoder which controls the output current of the CDCs, automatically controlling the frequency of the output signal.

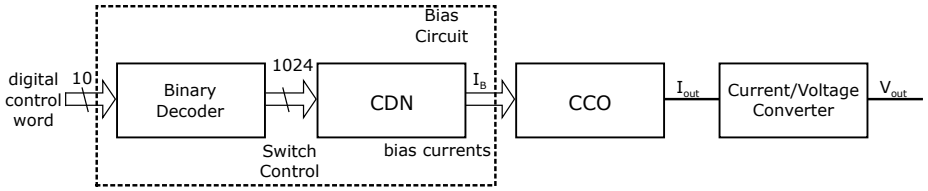

Fig. 4. Block schematic of the proposed DCO

3.1. Current Controlled Oscillator

The generalized structure of the CCO is presented in Figure 5.

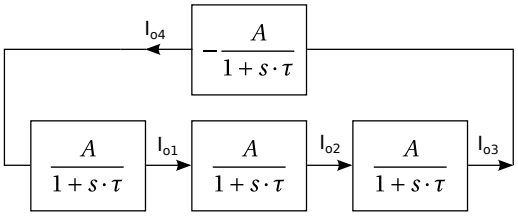

Fig. 5. Current controlled oscillator block schematics

It is based on the ring topology and consists of four integrator blocks, one inverting and three non-inverting current-mode log-domain integrators [17]. The output signals are currents and the output current of the inverting current-mode log-domain integrator is fed to the input of the first noninverting current-mode log-domain integrator. An even number of integrators are used in this design because modern communication systems require quadrature signals in their modulation stage. The transfer function of each integrator cell has the expression:

$$H(s) = \frac{A}{1 + s \cdot \tau} \tag{1}$$

where A is the dc gain and τ is the time constant of the integrator. In this case, the Barkhausen stability criterion, for the CCO from Figure 5 can be written as:

$$H(j\omega_0) = -\left(\frac{A}{1 + j\omega_0 \cdot \tau}\right)^4 = 1 \tag{2}$$

From (2) yields the expression for the oscillation frequency $\omega_0 = \frac{1}{\tau}$ and the minimum gain value for the circuit to oscillate $A = \sqrt{2}$. Each integrator is built using basic log-domain building cells: logarithmic cell, exponential current-sink cell and exponential current-source cell. These cells were implemented using CMOS transistors working in sub-threshold region. The electrical circuits and their symbols are presented in Figure 6. The output voltage of the logarithmic cell can be written as in (3) and the output current for the two exponential cells is given in (4).

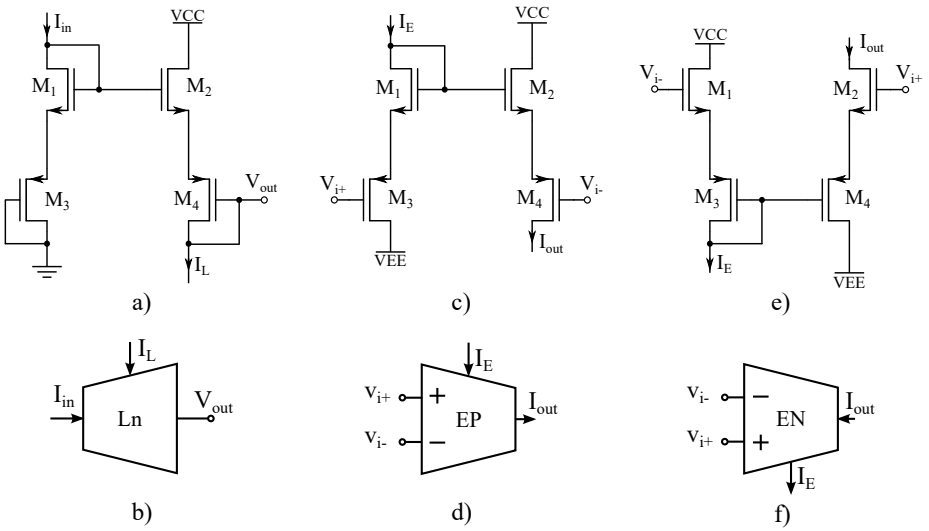

Fig. 6. Log-Domain basic building blocks: logarithmic circuit a) schematic view, b) symbol; exponential current source c) schematic view, d) symbol; exponential current sink e) schematic view f) symbol

$$V_{out} = 2 \cdot V_T \ln\left(\frac{I_{in}}{I_L}\right) \tag{3}$$

$$I_{out} = I_E \exp\left(\frac{V_{i+} - V_{i-}}{2 \cdot V_T}\right) \tag{4}$$

where V_T is the thermal voltage, I_L is the bias current of the logarithmic cell and I_E are the bias currents from the exponential cells. Using the cells from Figure 6 one can build the log-domain current mode noninverting integrator. This consists of one logarithmic cell (Ln), two exponential current-sink cells (EN_1, EN_2) and two exponential current-source cells (EP_1, EP_2). The block diagram is presented in Figure 7. For implementing the CCO one needs also an inverting current-mode log-domain integrator. This can be derived from the noninverting structure by connecting the capacitor to the positive input of the exponential current-sink EN_2 and the positive input of the exponential current-source EP_2 to the ground. The transfer function can be written as follows:

$$H(s) = \frac{i_{out}}{i_{in}} = \frac{\dfrac{I_E}{I_L}}{1 + s \cdot \left(\dfrac{2 \cdot V_T \cdot C}{I_{osc}}\right)} \tag{5}$$

Comparing the transfer function from (5) with the general form from (1), one can see that the gain can be adjusted using the ratio of the bias currents I_E and I_L while the time constant can be adjusted using the capacitor value and the bias current I_{osc}.

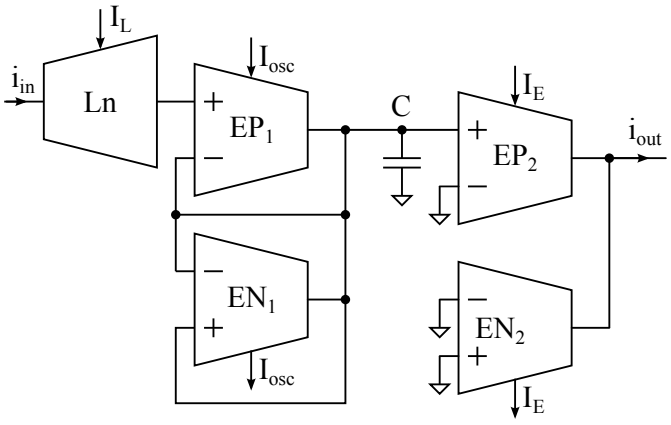

Fig. 7. Block diagram of the current-mode log-domain integrator

3.2. Bias Circuit

The role of the bias circuit, composed of a CDN and a binary decoder, is to provide the bias currents for the current-mode log-domain integrators. The CDN is implemented using CDCs (Figure 8). The number of CDC's is equal to the number of bias currents needed. For the CCO from Figure 5 one needs 3 CDC's, one providing the bias currents I_L for the logarithmic cells, one for the bias currents I_{osc} to control the time constant for the log-domain integrators and one to set the gain of the log-domain integrators by setting the value of the bias current I_E.

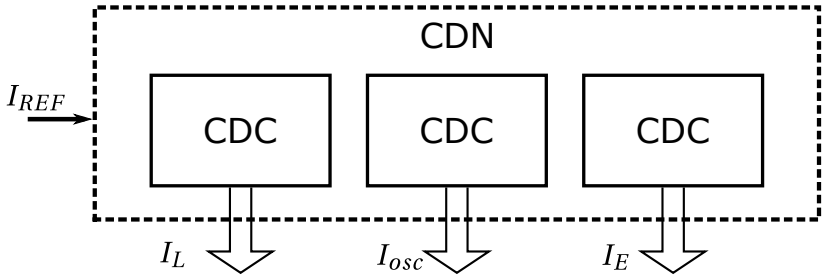

Fig. 8. Current Division Network

The CDC's were implemented using cascode current mirrors, using NMOS transistors, like the one presented in Figure 9, for biasing the logarithmic cells and the exponential current-sink cells. For biasing the exponential current-source cells one will need cascode current mirrors implemented using PMOS transistors. The number of output branches for every current mirror is equal to the number of desired bias current values. In this case, one needs four outputs for the CDC providing the bias currents for the logarithmic cells and eight output branches for the CDC providing the bias currents for the exponential current-sink and current-source cell which controls the gain of the current-mode log-domain integrators.

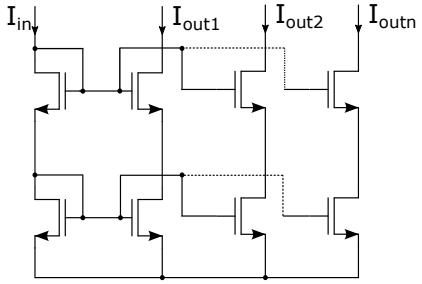

Fig. 9. Current Division Cell implemented using NMOS cascode current mirrors

The CDC providing the bias current which will set the current-mode log-domain integrator time constant needs to be programmable for tuning the frequency of the output signal. For this purpose, the CDC structure for the bias currents I_L and I_E was modified as in Figure 10.

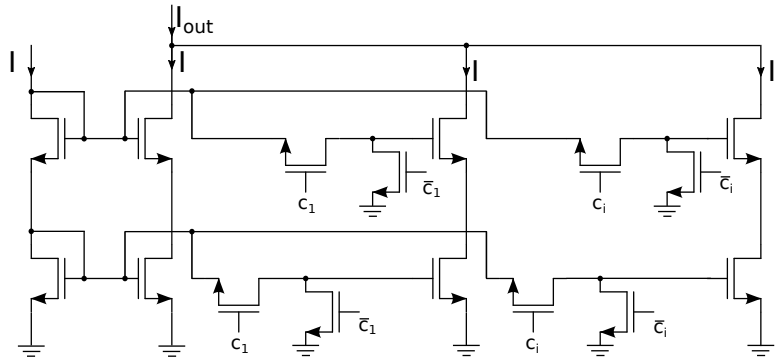

Fig. 10. Programmable current division cell implemented using NMOS cascode current mirrors

The outputs of the CDC can be turned on or off using MOS switches controlled by a digital control signal c. If the gain of the current mirrors are set to unity, the output current of the CDC can be written as in (6).

$$I_{out} = I + \sum_{i=1}^{1023} c_i \cdot I \tag{6}$$

For this CDC, the number of output branches, is equal to the desired resolution of the DCO. The implementation permits 1024 different frequency values. To obtain them, one needs a CDC with 8x1024 outputs, half of them coming from PMOS programmable current mirrors and the other half from NMOS ones. To change the bias current I_{osc}, which controls the time constant of the integrator automatically controlling the output signal frequency, one needs 1023 control signals. These signals are obtained using a binary decoder, presented in Figure 11. It consists of 1023 1-to-2 demultiplexers and 1023 OR gates. The 1023 control signals from the output are controlled using a 10 bit control word. The truth table of the binary decoder is presented in Table 1.

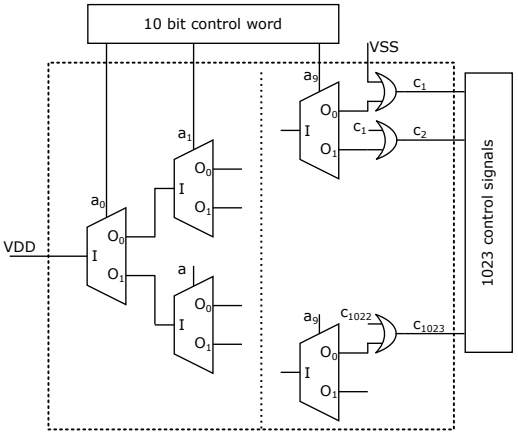

Fig. 11. Binary decoder block schematics

Table 1. Truth table of the binary decoder

control word					control signals						
a_9	a_8	$\cdots$	a_1	a_0	c_{1023}	c_{1022}	c_{1021}	$\cdots$	c_3	c_2	c_1
0	0	$\cdots$	0	0	0	0	0	$\cdots$	0	0	0
0	0	$\cdots$	0	1	0	0	0	$\cdots$	0	0	1
0	0	$\cdots$	1	0	0	0	0	$\cdots$	0	1	1
0	0	$\cdots$	1	1	0	0	0	$\cdots$	1	1	1
$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	
1	1	$\cdots$	0	0	0	0	0	$\cdots$	1	1	1
1	1	$\cdots$	0	1	0	0	1	$\cdots$	1	1	1
1	1	$\cdots$	1	0	0	1	1	$\cdots$	1	1	1
1	1	$\cdots$	1	1	1	1	1	$\cdots$	1	1	1

3.3. Current-Voltage Converter

The DCO output signal will be used as a clock signal for the next stage like presented in Figure 3 so, the output current of the CCO is converted to voltage. This is achieved using the CMOS current comparator from Figure 12 [18].

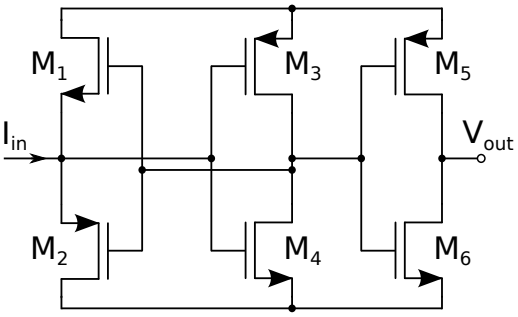

Fig. 12. Current-voltage converter

4. Simulation results

In order to demonstrate the operation of the proposed DCO, the constituent blocks (bias circuit, current controlled oscillator, curent-voltage converter) were implemented in Virtuoso Analog Design Environment from Cadence using a 180nm CMOS technology. The geometries of the CMOS transistors working in sub-threshold region were calculated for a maximum drain current equal to 2uA. This led to the following geometry ratios for the NMOS and PMOS transistors:

$$\begin{cases} \left(\frac{W}{L}\right)_{NMOS} = 46 \\ \left(\frac{W}{L}\right)_{PMOS} = 137 \end{cases} \tag{7}$$

The bias currents for the exponential cells which control the gain of the current-mode log-domain integrators (I_E) was set to 2uA so the bias current for the logarithmic cells (I_L) resulted 1.25uA. This way, the gain of every integrator cell was larger than $1/\sqrt{2}$. The input current of the CDC controlling the bias currents I_{osc}, which controls the oscillation frequency, was set to 10nA and the gain of the current mirror branches controlled by the control word a was set to 0.1. This way, the output current can be varied between 10nA corresponding to the control word a=$\{0000000000\}$ and 1034nA corresponding to the control word a=$\{1111111111\}$, with 1nA resolution. The integrating capacitor value (C) was set to 100fF.

Using Spectre Circuit Simulator simulations were performed. The figures 13 and 14 present the output signals resulted from transient analysis. The top graph represents the output of the current controlled oscillator and the one below the signal taken from the output of the current-voltage converter. The simulations were performed for $I_{osc} = 10nA$ (Figure 13) resulting a measured oscillation frequency equal to 90kHz and for $I_{osc} = 1034nA$ (Figure 14) resulting a measured oscillation frequency equal to 3.7MHz.

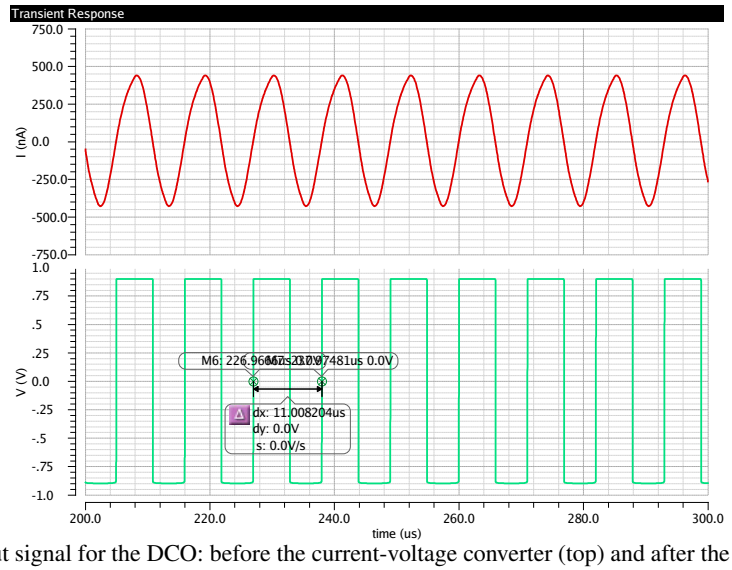

Fig. 13. Output signal for the DCO: before the current-voltage converter (top) and after the current-voltage converter (bottom) for I_{osc}=10nA

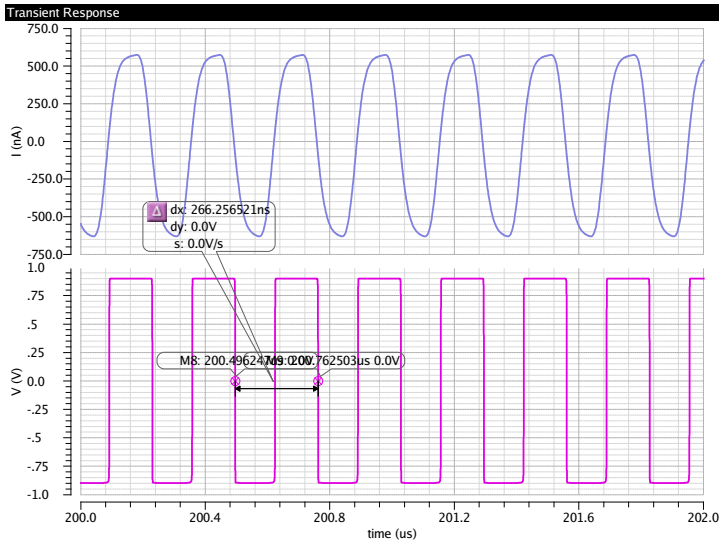

Fig. 14. Output signal for the DCO: before the current-voltage converter (top) and after the current-voltage converter (bottom) for I_{osc}=1034nA

Using this circuit it is possible to obtain quadrature output signals. In Figure 15 are presented the outputs I_{o1} and I_{o3} of the CCO from Figure 5 (top) and their voltage counterpart obtained using two current-voltage converters for an I_{osc} corresponding to the control word a=$\{1111111111\}$, equal to 1034nA. The measured delay between the signals correspond to a phase shift equal to 92^o. In Figure 16, the DCO tuning with respect to the bias current I_{osc} is presented. On the horizontal axes we have the bias current values I_{osc} corresponding to the control word a ranging from 10nA to 1034nA and on the vertical axes we have the frequency values obtained for these current values.

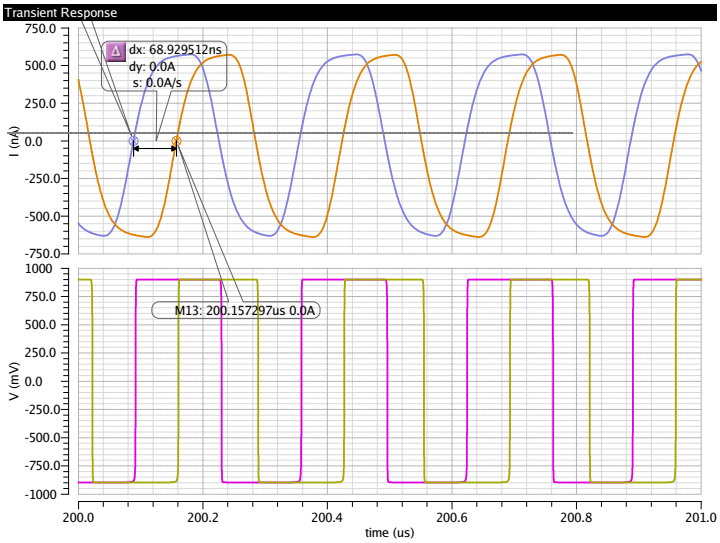

Fig. 15. Quadrature output signals for the DCO: before the current-voltage converter (top) and after the current-voltage converter (bottom) for I_{osc}=1034nA

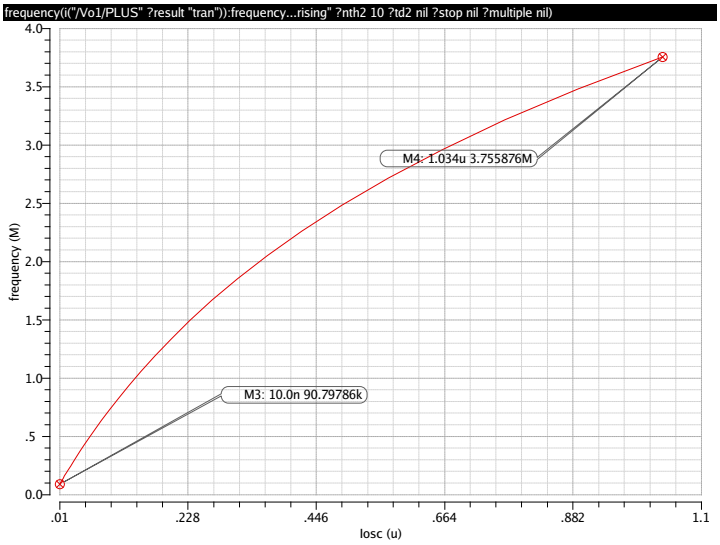

Fig. 16. Measured oscillation frequency versus bias current I_{osc}

Figure 17 shows the phase noise of the presented DCO. The phase noise is -66dBc/Hz at a 10kHz offset and -88dBc/Hz at 100kHz offset when the output frequency is 1MHz.

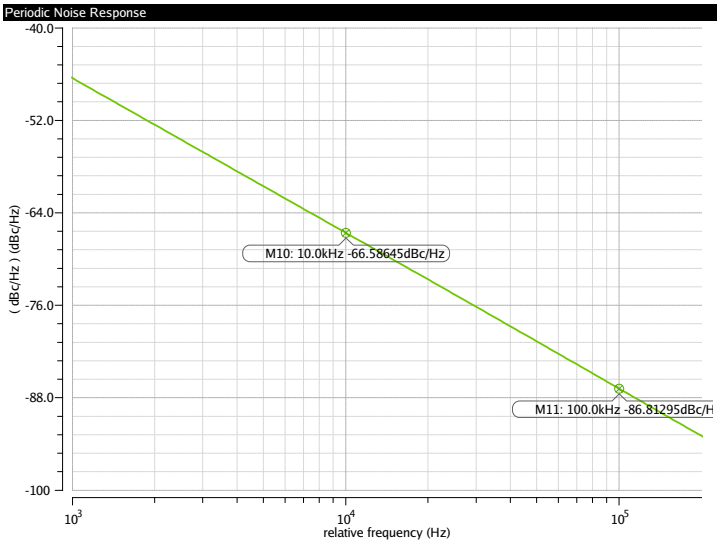

Fig. 17. Simulated Phase Noise for f_{osc}=1MHz

Table 2 compares low voltage VCOs and DCOs in terms of their performance. The proposed architecture has the largest tunning range.

Table 2. Comparison with other works

	VDD	Technology	Frequency range	Power	Phase noise
This work	1.8V	180nm	0.09 - 3.7 MHz	105 uW	-88dBc/Hz@100kHz
RFIT'15 [5]	0.7V	130nm	382 - 412 MHz	840 uW	-115dBc/Hz@100kHz
TCAS'13 [7]	0.5V	90nm	0.16 - 1.5 GHz	1157 uW	-87dBc/Hz@1MHz
TCAS'09 [8]	0.5V	130nm	306 - 725 MHz	210 uW	-95dBc/Hz@1MHz
JSSC'05 [4]	0.5V	180nm	3.6 - 3.9 GHz	570 uW	-119dBc/Hz@1MHz
SSCC'13 [6]	1.2V	180nm	12.6 MHz	98 uW	-120dBc/Hz@1MHz

5. Conclusion

In this paper, a novel implementation of a digitally controlled oscillator is presented, emphasizing its deployment in all digital phase/frequency locked loops. It is based on the ring topology and consists of four log-domain current-mode integrators. Using this implementation, the frequency can be tuned using the bias currents. The bias currents are obtained using a binary decoder and a current division network. The binary decoder role is to generate the control signals for the switches inside a current division cell. A 10-bit control word was used to generate 1024 control signals which in turn conducted to 1024 current values and 1024 distinct frequencies. The reported DCO was implemented in Virtuoso Analog Design Environment from Cadence using a 180nm CMOS process technology. To demonstrate the operation, Spectre simulations were performed. They show that the proposed DCO has a frequency tuning range from 90kHz to 3.7MHz and it is possible to obtain quadrature signals. The power consumption for f_{osc}=1MHz is 105uW. The simulated phase noise at 100kHz offset frequency is -88dBc/Hz. Further work is focused on silicon implementation, in order to prove the presented approach.

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