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Investigations of the Fabricated Nothing On Insulator Nanodevices as Metal-Air-Metal variant - NOI-MAM

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Abstract. This paper presents some investigations of an experimental Nothing On Insulator device, made in the Metal-Air-Metal (NOI-MAM) variant. The vacuum nanodevices are potential candidates for tera-Hertz applications. The investigations concern the fabrication processes, measurements of the output characteristics and simulations of the NOI-MAM devices. Two metallic nanowires are considered instead of two semiconductor nano-islands for Source and Drain. Air molecules in normal conditions inside a gap of maximum 36 nm size represents the "Nothing" area. The electron-beam lithography technology or AFM sectioning by tips are investigated by SEM and AFM analysis. The measured and simulated current-voltage curves are investigated for potential applications.

Key-words: Nanotechnology; Metallic nanowires; electron-beam lithography; vacuum devices; SEM, AFM.

1. Introduction

In recent years, the nano-wire transistors and vacuum field effect nano-transistors [1-3], offered benefits like tera-hertz operation [4], low power and carriers transport without scattering.

Ballistic transport occurs in nanotubes or in air nano-cavities sub-65 nm length, as in vacuum conditions, [5].

The classical vacuum diodes and triodes possess high sizes, even in 1999 year [6], or later [7]. The fabrication of the vacuum nano-devices represents a new challenge. Their main applications seem to be the frequency gap filling between 10 GHz and 10 THz, [8]. The Nothing On Insulator (NOI) transistor [9] belongs to this devices class of international interest. Its fabrication in silicon was patented in 2013 [10]. NOI device optimizations occurred only by simulations [11-13]. In 2018, some authors who cited our previous work [12], reported a nano-scale field emission transistor with an average air gap of 30 nm [5]. They used different metallic compounds to fabricate extremely thin tips from Gold or Tungsten, [5]. If the tips are fabricated as metallic nanowires on thin oxide grown on a Si-wafer, this structure becomes a NOI-MAM variant, as Nothing On Insulator device in the Metal-Air-Metal variant, instead of semiconductor-nothing-semiconductor [12], as successive Drain-Source materials. In 2013, the NOI device with metals instead semiconductors was discussed [14, 15]. Till 2020, its variants were only investigated by Atlas simulations, [15, 16]. A recent publication from 2020 of our team demonstrated for the first time the NOI-MAM fabrication with metals islands instead source-drain semiconductor islands, [17]. The drain current modulation doesn't occur under a gate action, accordingly with previous experiments [17] and separate simulations [18-21]. Therefore, this paper is focused rather on further investigations.

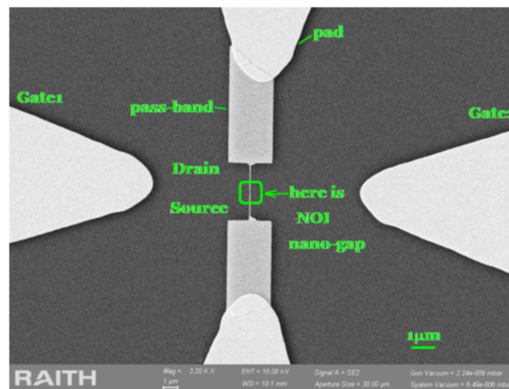
The novelties of this paper concern: emphasizing the Electron Beam Lithography (EBL) as the primary suitable technology, a secondary method investigated by AFM, additional simulation results of the functionality and non-linear electrical conduction between Source-Drain inside this NOI-MAM variant.

2. NOI-Technology investigations

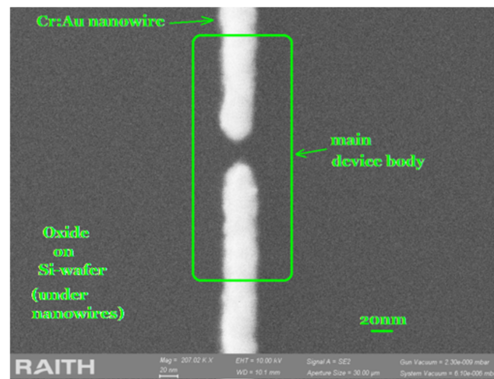
2.1. SEM Investigations

The technological flow was largely depicted elsewhere [17, 21]. A short description starts from an oxide film 1.5 μm thickness. It is grown on Si-wafer <100>, 5 Ω.cm resistivity. By sputtering, two metallic nanowires of Cr:Au are deposited in high vacuum. The role of Cr is for adhesion to oxide. These nanowires are essentially the metallic Source and Drain of the NOI-MAM variant. The nanowire shape was configured by lift-off process.

Besides to Source - Drain nanowires, some metallic pads of $10\mu m \times 10\mu m$ are gradually contacted to other two pass-bands, Fig. 1a. Additional two transversal metallic Gate1-Gate2 pads are created to investigate potential current modulation under the Gates action, Fig. 1.a. In a recent analysis, this feature was invalidated, because the Source-Drain electric field inside the air-gap is thousands time stronger than the Gate1-Gate2 electric field, [21]. As an initial technological exercise, the Source-Drain pass-pads of $2.5\mu m \times 10\mu m$ are also defined by Electron Beam Lithography (EBL). Finally, the nano-lithography of both Cr:Au nanowires is achieved by EBL nanoengineering workstation. Between nanowires, three gaps are configured. A PMMA photoresist of 50 nm thickness is spin-coated. After exposure and developing, the sputtering deposition of Cr-5 nm and an Au-35 nm deposition occur. The nanowire locations are etched in PMMA by EBL, providing three NOI variants: NOI1, NOI2 and NOI3. In PMMA, the nanowire gap has 24 nm for NOI1, 28 nm for NOI2 and 36 nm for NOI3, as Stage-a, Fig. 2.



(a)



(b)

Fig. 1. (a) The SEM image of the fabricated NOI device, in MAM variant, getting possible transversal electrodes for Gate1/Gate2; (b) detail: the encircled zone stands for the main NOI-MAM device body with Source and Drain nanowires on oxide surface.

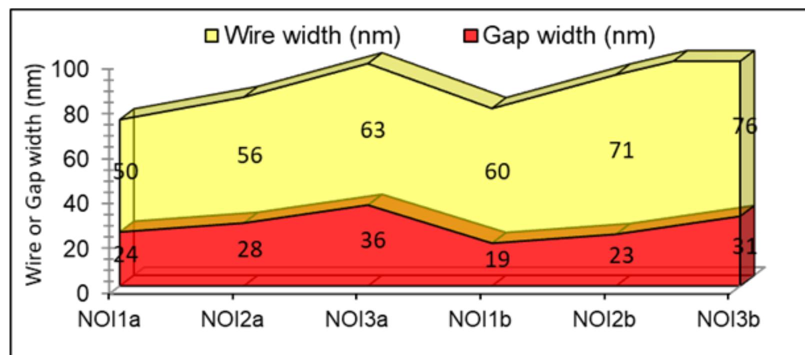


Fig. 2. The main sizes of the NOI1, NOI2 and NOI3 devices after Stage-a and after Stage-b. For instance, notation NOI2a means the NOI2 structure after Stage-a.

Subsequent lift-off process in acetone configured lower gap between nanowires, because the metals overfilled the graved places. In this final Stage-b, the Source-Drain nanowires of 50 ... 70 nm width and 3 μm length are separated by a middle gap: 19 nm for NOI1, 23 nm for NOI2 and 31 nm for NOI3. A gap detail for the NOI2 device is presented by SEM, after EBL and lift-off in Fig. 1b. Figure 2 contains the width of the gaps after the nano-lithography process (structures NOI1a, NOI2a, NOI3a) and finally after lift-off, for the same structures, but at Stage-b (structures NOI1b, NOI2b, NOI3b).

2.2. AFM Investigations

In this section, a distinct technological solution is envisaged, to achieve a gap inside a long nanowire. The previous technological steps from Section 2.1 are repeated to define a continuous nanowire between the Source and Drain contacts, except any etching process, fig. 3. The nanowire structure takes similar size to the previous NOI variant, [17].

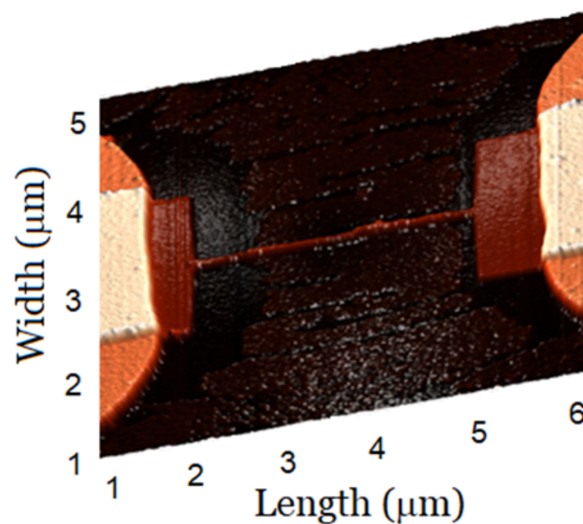


Fig. 3. AFM image of a long nanowire in connection with two lateral pads.

The AFM probe-tips were used to scratch this nanowire, in order to investigate possible lower gap between two adjacent nanowires. This scratching technique was used by other authors, too, [22, 23].

Figures 4 illustrates the result of the nanowire sectioning by AFM tip, sacrificing a peak of AFM. More tests are necessary to correctly evaluate the tip pressure, since a complete separation between the Source and the Drain island. Obviously, a more accurate AFM measurement of the separation region between the Source and Drain nano-wires, is possible with an infinitely thin and narrow peak of the tip, because the geometry of the peak influences the measurement resolution [24]. In this regard, the virtual profile along the sectioned line, which reproduces to some extent the shape of the peak, is available in Fig. 5. The actual method is more suitable to produce an almost a-NOI device [10], in a future study.

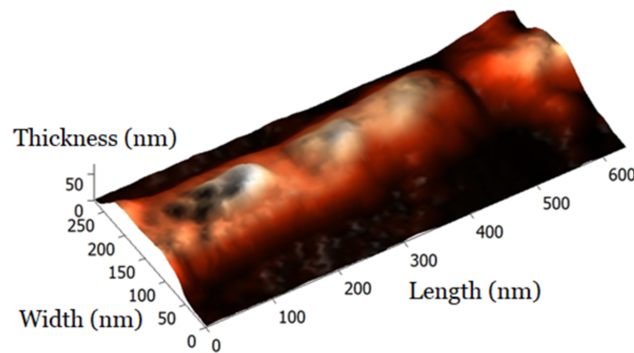


Fig. 4. Detail of an AFM image: scratching a long Au:Cr nanowire.

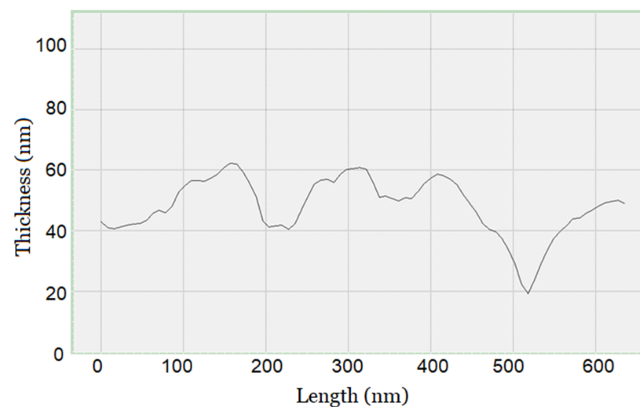


Fig. 5. The metallic nanowire profile along the sectioned line by the AFM peak.

During the scratch method, it would be expected that the Cr layer remains on the surface. This is verified by Fig. 5. In this case, the measured I_D-V_{DS} curve presents linear dependence like a resistor, before melting.

3. Experimental investigations

The fabricated device has an air-gap instead a vacuum-gap. But, these two situations are quite equivalent. Further vacuum expensive techniques are not necessary to be applied. This Air-Gap NOI variant has the advantage to be a nanoscale device. At room temperature, the mean free path of the electrons in air is sub-65 nm [25]. Consequently, the an air-gap under 36 nm can be admitted as a vacuum gap, serving the scope of a Nothing On Insulator device.

Firstly, the output characteristics of the fabricated NOI-MAM devices are recorded. The Drain-Source voltage is applied from a DC power supply, while the drain current is measured by a Keithley 6847 Pico-ammeter. The measured I_D-V_{DS} characteristics of the NOI1 and NOI2 variants are presented in Fig. 6. The NOI1 variant suffers from stacks depositions inside gap [17], with a peak current at +1 V, Fig. 6.

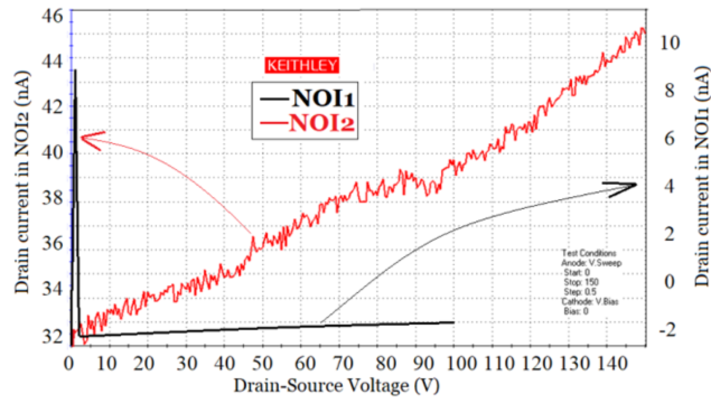


Fig. 6. The I_D-V_{DS} measured characteristics for NOI1 and NOI2 devices.

Figure 7 presents the comparison among different static characteristics picked from literature and the characteristic of the actual NOI-MAM device. The compared devices are: our NOI3 variant, Metal-Air Field Emission nano-Transistor (MAFET) [5], Si-Semiconductor Vacuum Nanotransistor (SVN) [14] and Metal-Insulator-Metal (MIM) structure [26].

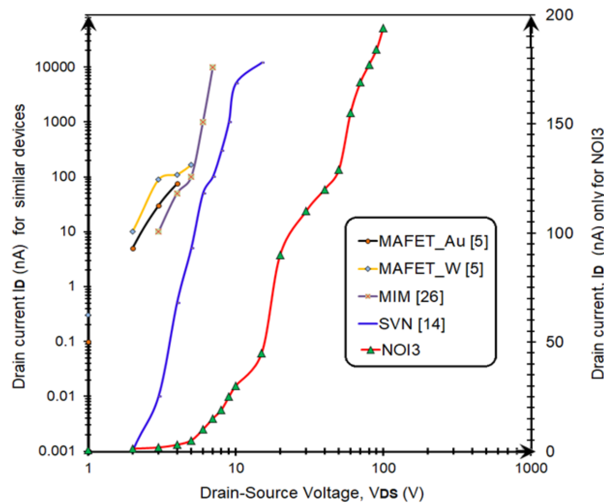


Fig. 7. Comparison of the measured I_D-V_{DS} characteristics of our NOI3 variant on right side, with picked points from similar experimental devices [5, 14, 26].

Figure 7 presents on the right side only the drain current at linear scale, of the NOI-MAM device in NOI3 variant. On the left side, the drain currents of three distinct related nano-devices [5, 14, 26] are presented at logarithmic scale. For all the devices, the drain current increases with the drain voltage. The closest I_D-V_{DS} characteristics occur for NOI3 and vacuum nanotransistor SVN [14]. The Metal-Insulator-Metal quantum tunneling for sub-30 nm air gap occurs both for MIM devices [26] and NOI3 [17].

4. Investigations by simulations

A previous analysis was related to the electric field simulation across the NOI-MAM structure, which proved a null electric field inside the metallic nanowires, [18]. Under the Gate biasing, no carriers modulation occurred, due to the thick oxide under experimental Cr/Au nanowires [17]. Thinner oxides suffer from oxide breakdown [21]. Therefore, an appropriate NOI-MAM variant with similar features as experimental device is simulated in Atlas/Silvaco, in this section. The investigations are directed rather to I_D-V_{DS} non-linear characteristics than to transfer characteristics that are inexistent. The input file for simulation considers: 40 nm Au nanowires for Source and Drain placed on 1.5 μm oxide, a default size of 1 μm on Oz axis for all materials and 20 nm air gap for NOI1, 25 nm for NOI2 and 30 nm for NOI3. Following models are used: Fermi distribution for electrons in any material, Metal-Insulator-Metal tunneling activated by MIMTUN statement, lattice temperature and heating - activated, room temperature of 300 K for the starting point of the device simulation.

Figure 8 a, b presents the electric field in different zones from the NOI-MAM device, variant NOI1, so that the image can keep the visibility proportions. The NOI-MAM device is biased at V_{DS} = 50 V, V_{GS} = 23 V, as average values of the experimental tests. The simulations reveal a potential gradient beneath oxide up to 70 nm at these voltages, Fig. 8a. Inside the active device area - the “Nothing” region near insulator, we observe two peaks of the electric field up to 3.3×10^7 V/cm demonstrating that appropriate conditions exist for the air-gap tunneling, at this drain voltage, Fig. 8b.

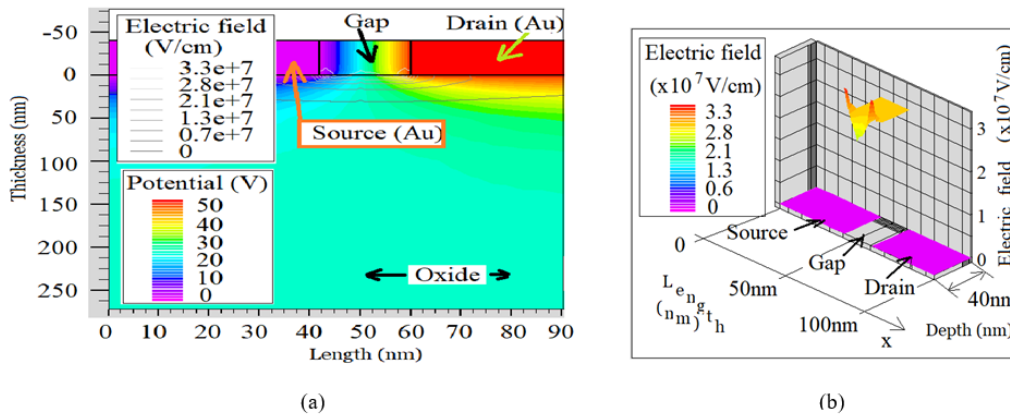


Fig. 8. (a) The electric field lines across the entire NOI-MAM structure; its biasing is provided by the color code; (b) detail of the electric field inside the active zone of the device at V_{DS} = 50 V, V_{GS} = 23 V.

In previous experiments, the useful Drain-Source tunneling was suspected to be perturbed by secondary effects [17], like local melting, nanowires interruptions or nano-structure heating at these small sizes, as other authors reported [5, 14, 27]. Hence, the lattice temperature simulations are performed in the actual work. If the thermal heating occurs near the metals-air corners, a strong temperature gradient arises inside the top electrodes, Fig. 9. As experimental measurements predicted, the Drain-Source electrodes heating occurs at V_{DS} = 50 V up to 1000 K, accordingly to Fig. 9. Therefore, the future theoretical models for the static characteristics of the NOI-MAM devices must take care on the thermal effects, too.

Comparisons of the I_D-V_{DS} curves for the experimental vacuum nanodevices and simulated NOI-MAM structure were still investigated from previous papers [17, 18, 21]. The next figure presents the simulation results of the I_D-V_{DS} curves for three distances of the air-gap inside the NOI-MAM variants: NOI1, NOI2 and NOI3, close to the fabricated NOI-MAM structures.

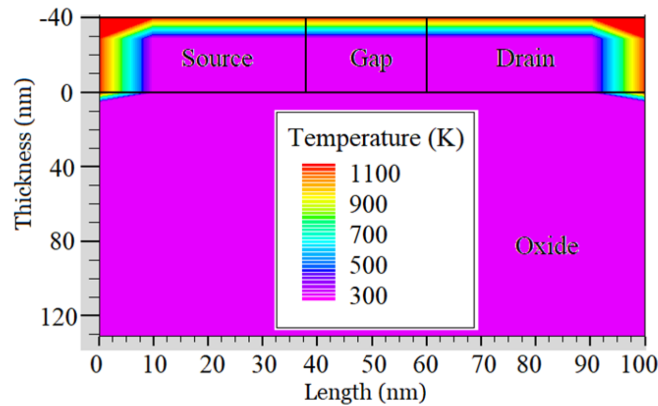


Fig. 9. The simulated temperature distribution inside the NOI-MAM variant - detail at the surface region.

In this analysis, a conventional drain current of 0.01 A can define some drain threshold voltages. For different NOI-MAM devices, the following threshold voltages result: 19.2 V for NOI1, 22.9 V for NOI2, 29.1 V for NOI3, Fig. 10a. Figure 10b shows a detail from these curves, only in the region where they are quite distinct, for 16 V $< V_{DS} <$ 26 V.

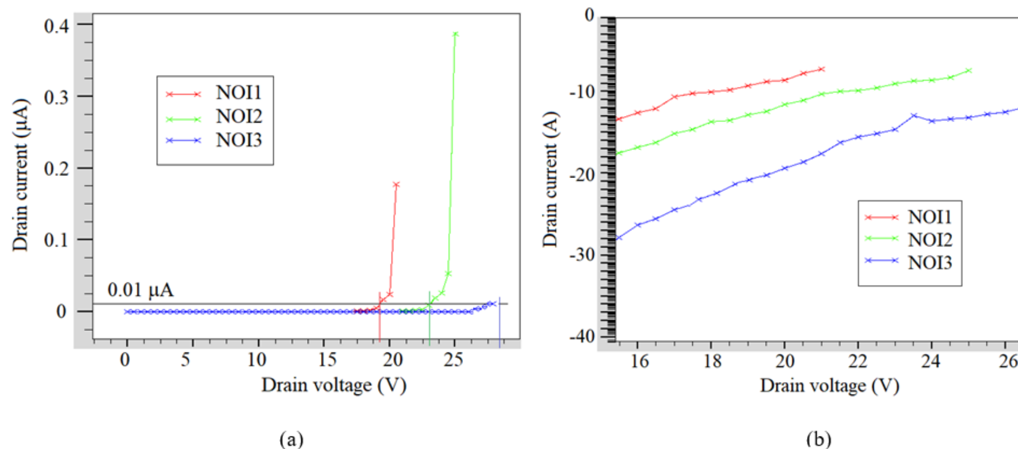


Fig. 10. The I_D - V_{DS} curves for the simulated NOI-MAM devices with air-gap of NOI1, NOI2 and NOI3, biased to V_{GS} = 1 V and variable V_{DS} at: (a) linear, (b) logarithmic scale.

The simulation results indicate that a potential application of the NOI-MAM device is as a nanoscale diode using I_D - V_{DS} exponential curves.

Differences exist between simulated curves from Fig. 10 a-b and experimental curves from

Fig. 6. An explanation can be the thermal regime that accompanies the real electrical tests. To attenuate the nanostructure self-heating during the device biasing, a maximum dissipated power is established. Reference [28] indicates the specific heat - 128 J/Kg·K for Au, 450 J/Kg·K for Cr, a melting temperature over 1335 K for Cr/Au and evacuation thermal conductivity of the oxide substrate of 0.014 W/cm/K. Therefore, the maximum power at Drain-Source voltage, for each NOI-MAM structure results: NOI1 - 105 nW at V_{DS}=10 V, NOI2 - 190 nW at V_{DS}=20 V and NOI3 - 222 nW at V_{DS}=35 V. These values can explain the current peak from Fig. 6 for the NOI1 device, when $V_{DS} < 10$ V, by a phase transition.

An Ultra Low Power Diode (ULPD) based Differential Cascode Voltage Switch Logic (DCVSL) circuit using NOI devices, represents a separate application. ULPD must be a combination of NOI and MOS transistors. By replacing a resistor with a ULPD, parasitic effects and the propagation times $T_{PLH}>T_{PHL}$ can be minimized [29].

5. Conclusions

An air-gap nano-device, noted by Nothing On Insulator Metal-Air-Metal NOI-MAM variant, was investigated. Two technological tests were considered: (i) EBL process that provided gaps between two adjacent Au:Cr nanowires of 19 nm, 23 nm and 31 nm; (ii) AFM scratching of a long Au:Cr nanowire, sacrificing the AFM probe. The separation of the Source and Drain nanowires were not complete for the AFM scratching method. But this last method is suitable for future fabrication of almost-NOI devices, which require an ultra-thin link channel between Source and Drain nano-islands. The investigated NOI-MAM devices presented increasing drain current with drain voltage, as majority of the related nano-devices. The simulations in Atlas of the NOI1, NOI2 and NOI3 variants indicated possible applications in Differential Cascode Voltage Switch Logic DCVSL, using CMOS co-integration with NOI-MAM devices instead resistances or pn junctions.

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