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Enhanced Method of Schottky Barrier Diodes Performance Assessment

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Abstract. An elaborate characterization of Si Schottky diodes, fabricated with Ti and Mo contacts, is presented. Thermal treatment in forming gas is performed in order to improve the electrical performance of the fabricated samples. X-ray diffraction measurements show the presence of different metal silicides after the annealing. Contact inhomogeneity is confirmed following an electrical characterization over a wide temperature range (15-500K) for both types of Schottky diodes. Conventional parameterization demonstrates a variation with temperature for the main electrical parameters of a Schottky diode (ideality factor and Schottky barrier height). At least two Gaussian distributions of barriers on the contact surface are evinced by using a standard inhomogeneity model. In our case, this approach is limited to a temperature range of 25-200K. In order to assess the devices' behavior over a wider temperature range, our *p-diode* technique is used. According to it, each experimental sample is demonstrated to behave as three nearly ideal diodes connected in parallel. Thus, model-fitted curves are in excellent agreement with measurements in a temperature range of 60-500K. The comprehensive characterization techniques are able to identify Schottky diode sample performance over their entire operational domain.

Key-words: Forming gas; inhomogeneity; metal silicides; *p-diode* model; Schottky barrier diode.

1. Introduction

Technologically, the simplest solid-state electron structures that can be fabricated are *metal/ semiconductor* (M/S) contacts, which are intensively used in achieving electronic devices. Depending on metal type and thermal treatment, either rectifying (Schottky) or resistive (Ohmic) contacts may be obtained. Over time, different metals were used as Schottky/ohmic contacts on Si or SiC substrates, such as Ni [1], Ti [2] or Pt [3]. Their use in electronic devices depends on the targeted application. For *Schottky barrier diodes* (SBDs) in switching applications, a metal with a low work function (WF) is desirable, such as Ti or Mo, in order to achieve better energy efficiency in conduction. Alternatively, if high-temperature operation is required, metals such as Ni, with a larger work function are more suitable. Usually, *post-metallization annealing* (PMA) [1, 4, 5] is performed, in order to produce devices with more stable electrical characteristics, through the formation of silicide phases at the M/S interface. However, even with such treatments, contact inhomogeneity still occurs, affecting one of the devices most significant parameter, the *Schottky barrier height* (SBH) [6]. For this reason, assessing a Schottky diode's effective performance still represents a challenge, despite the devices being investigated for over fifty years [7, 8]. In order to unravel the electrical behavior for these types of contacts and to identify the main conduction mechanism, electrical measurements over a wide temperature range must be performed, followed by extensive parameterization of the resulting characteristics.

In this paper, the fabrication and electrical characterization of Ti/Si and Mo/Si Schottky barrier diodes are presented in a wide temperature domain (15 – 500K). Section 2 gives details about the technological processes. The effect of PMA treatment, performed in *forming gas atmosphere* (FGA), for each fabricated sample is discussed in Section 3. The results represent an extension of those evinced in [9]. In order to obtain information about the metal silicide formation and overall contact quality, microstructural investigations by means of *X-ray diffraction* (XRD) are carried out. In Section 4, following conventional analysis of experimental forward curves over the entire temperature interval, the presence of contact inhomogeneity is confirmed. As such, specialized models are used in order to establish the performance of the samples and their optimum operating temperature domain. In particular, our recently proposed *p-diode* model was able to fully explain forward electrical behavior in the 60 – 500K range. Finally, conclusions are drawn in Section 5.

2. Experimental Details

The Schottky diode samples were fabricated starting from heavily doped (10^{19} cm^{-3}) n-type Si wafers with a 10μm epitaxial layer ($5{\cdot}10^{14}$ cm^{-3} doping). Initially, the wafers were chemical cleaned using the standard RCA recipe [10] in order to prepare them for the surface processing. A first technological process for surface passivation was performed, based on a *Low Pressure Chemical Vapor Deposition* (LPCVD) technique, consisting in 600nm SiO_2 thickness deposited on the front side of the Si wafers. In this field oxide, the active areas of Schottky barrier diodes were achieved using standard photolithographic processes. The structure layout contains two identical Schottky contacts, having a circular geometry with a diameter of 400 μm [9]. In order to obtain the ohmic contacts for our devices, a successive metal deposition was performed on the backside of the Si substrate, consisting in Ti (100 nm)/Al (300 nm). For the Schottky contacts, two different metals were deposited on the wafers' frontside: Ti (100nm) and Mo (100nm). In order to define the pad contacts of the final structures, 300nm of Al were deposited over the Schottky contacts. These metals were defined using standard photolithography in the field oxide.

A PMA treatment in forming gas atmosphere (450°C, for 30 minutes) was performed for some samples. Consequently, four different SBD types were obtained: a) unannealed Ti contact (*Ti*), b) annealed Ti contact (*Ti-FGA*), c) unannealed Mo contact (*Mo*), d) annealed Mo contact (*Mo-FGA*). The samples, depicted in Fig. 1a), each containing two SBD structures, were diced and encapsulated in TO39 packages using wire-bonding technology. I-V characteristics of the packaged samples were measured at different temperatures, between 15–500K, using a Keithley 4200 semiconductor characterization system coupled with a Janis closed cycle refrigerator system illustrated in Fig. 1b).

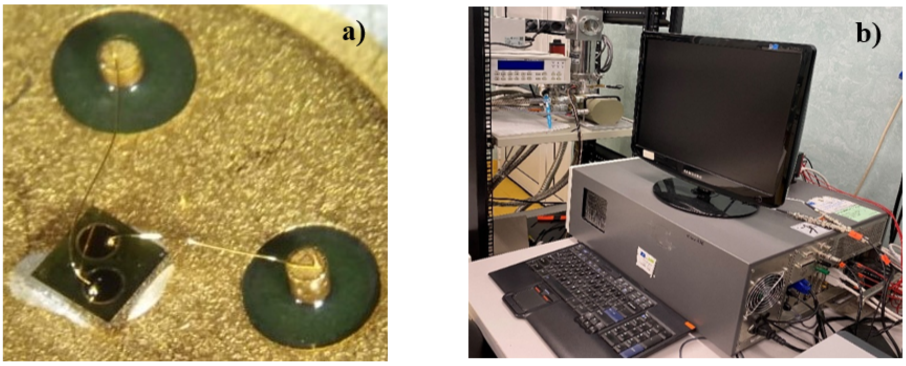

Fig. 1. a) Samples packaged using wire bonding technology; b) the I-V-T measurement system.

3. Microstructural Investigations

The microstructure of the samples was investigated using XRD technique using a 9kW Rigaku SmartLab diffraction system with rotating anode, equipped with a Cu-K1 radiation source ($\lambda = 1.5406$Å), operated at 40kV and 75mA. The patterns were recorded in 2θ range of 20–90° at a scanning rate of 8° $\min^{-1}$ and with a 0.01° step width. Identification of crystalline phases was realized using standard *International Centre for Diffraction Data* (ICDD) database. Analysis of the resulted films was performed in order to reveal the phase composition as displayed in Fig. 2.

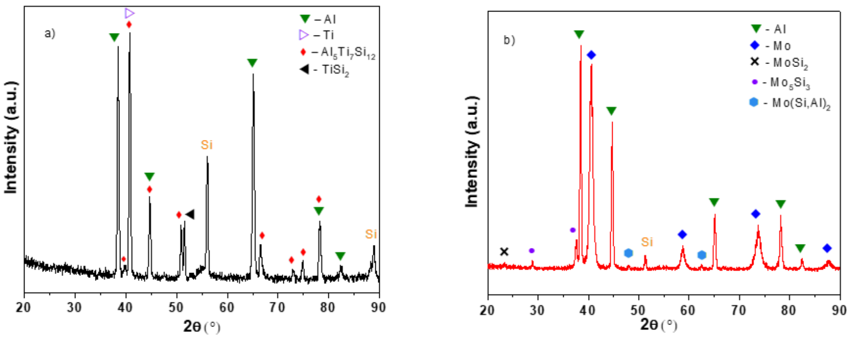

Fig. 2. XRD patterns for the annealed samples: a) *Ti-FGA*; b) *Mo-FGA*.

The XRD pattern for the *Ti-FGA* sample (Fig. 2a)) exhibits diffraction peaks ascribed to Si substrate (JCPDS card no. 01-7247) corresponding to (311) and (422) atomic planes at $2\theta = 56°$ and 88.8°. Those of metallic Al at $2\theta = 38.5°$, 44.7°, 65.2°, 78.3° and 82.3° correspond to (111), (200), (220), (311) and (222) atomic planes of Al (ICDD card no. 01-1176) and Ti phase at $2\theta = 40.9°$ for the (101) atomic plane of Ti (ICDD card no. 01-1198). Therefore, the additional peaks located at $2\theta = 39.8°$, 50.9°, 66.5°, 72.9° and 74.9°, confirm the formation of an alloy containing all the elements of the sample (Al, Ti and Si atoms), whose plane reflections can be attributed to $Ti_7Al_5Si_{12}$ phase (JCPDS card no. 018-0071) with (00 12), (10 13), (20 12), (11 18) and (220) atomic planes. At the same time, there is some overlapping of the most intense lines of the $Ti_7Al_5Si_{12}$ phase, which can be ascribed to the (116), (10 11) and (10 21) atomic planes with those of Al and Ti at $2\theta = 40.9°$, 44.8° and 78.3°, respectively. The presence of a diffraction line at $2\theta = 51.5°$ reveals formation of another alloy, which is assigned to the (002) atomic plane of $C_{49}TiSi_2$ (ICDD card no. 04-002-1352). Moreover, the annealing process favor the diffusion of Si atoms into the metallic Al and Ti phases, forming different alloy phases, as evidenced from the XRD pattern. Similar results were reported in [11, 12]. The XRD analysis of the *Mo-FGA* sample exhibits well-defined diffraction lines of Al phase that can be observed at $2\theta = 38.5°$, 44.8°, 65.2°, 78.3° and 82.5°, corresponding to (111), (200), (220), (311) and (222) atomic planes of Al (ICDD card no. 01-1176). Those of Mo phase are located at $2\theta = 40.6°$, 58.7°, 73.6° and 87.7° for the (110), (200), (211) and (220) atomic planes of Mo (ICDD card no. 01-1205). The annealing process favored the formation of Mo_5Si_3 with diffraction lines at $2\theta = 28.8°$ and 37.6°, $Mo(Si, Al)_2$ with peaks at $2\theta = 48°$ and 62.4° and $MoSi_2$ at $2\theta = 23.4°$. Recently, similar results were obtained in [13, 14].

4. Electrical Characterization

4.1. Temperature dependent electrical characteristics

Figure 3 shows typical forward and reverse bias I-V characteristics of fabricated samples in the temperature range of 15 – 500K.

It is evinced that, although all diodes exhibit some form of exponential current-voltage dependence in forward bias, the I-V characteristics of annealed devices (*Ti-FGA* and *Mo-FGA*) have more uniform profiles. The better behavior of these devices is also confirmed in the reverse bias region, where the leakage currents are much lower and more stable than those of their unannealed counterparts. Conversely, the *Ti* diode shows (Fig. 3a)) an almost ohmic behavior, with very high reverse-bias currents, especially above 300K. Also, in the forward-bias region, the dense grouping of the I-V characteristics indicates an abnormally low barrier height. Whereas this behavior is not as pronounced for the unannealed *Mo* sample, it also exhibits irregularities on the forward characteristics, coupled with leakage currents at least one order of magnitude higher than its *Mo-FGA* counterpart.

Thus, the FGA-devices (*Ti-FGA* and *Mo-FGA*) were selected for further characterization in order to confirm their superior performance.

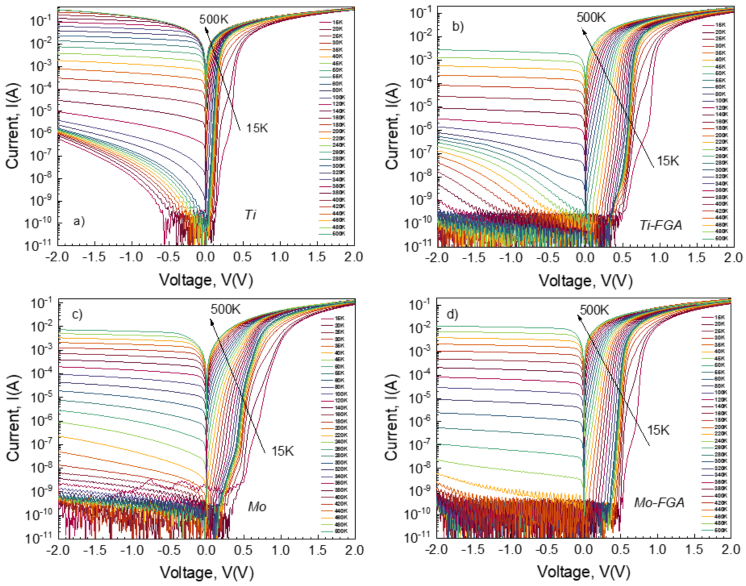

Fig. 3. Experimental forward and reverse bias I-V characteristics of the SBDs at various temperatures.

4.2. Conventional method for SBD characterization

The *thermionic emission* (TE) law governs the I-V-T characteristics of an ideal SBD [15–19]:

$$I_F \cong I_S \text{exp}(\frac{V_F - I_F R_S}{nV_{th}}), \tag{1}$$

where R_S is the series resistance, n is the ideality factor, $V_{th} = kT/q$ is the thermal voltage and I_S is the saturation current:

$$I_S \cong A_n A_S T^2 \text{exp}(-\frac{\Phi_{Bn,T}}{V_{th}}). \tag{2}$$

In (2), according to the design of A_S representing the nominal contact area, A_n is the Richardson constant for electrons (112 A/K^2 cm^2 for n-type Si), and $\Phi_{Bn,T}$ is the conventional *Schottky Barrier Height* (SBH).

The most common method to determine the electrical parameters of a Schottky barrier diode is based on a linear fit of the ln(I_F) as a function of V_F plot [15]. According to the TE theory, a homogenous Schottky contact should exhibit a SBH and ideality factor independent on voltage and temperature. These parameters, alongside saturation current and series resistance were extracted for both *Ti-FGA* and *Mo-FGA* diodes at each temperature (Fig. 4), in order to determine the temperature range and bias domains, where they exhibit nearly ideal electrical behavior.

The investigated temperature domain enables identifying the limits of the TE conduction mechanism in the samples. At low temperatures, the effects of carrier freeze-out and weak ionization [20] become prominent, yielding the forward anomalous curves in Figs. 3b) and 3d) (below 60K). Similarly, as the operation limits of Si are reached at high temperatures (above 440K), the effects of the series resistance overtake the exponential I-V dependence. For diodes with relatively uniform contacts, the ideality factor should exhibit values close to unity. For both investigated SBDs, this occurs in the 160 – 300K temperature interval, where n is between 1.01 and 1.1. This range is also associated with a stable value for the Schottky Barrier Height. On the other hand, significant temperature dependence for these parameters was determined in the 60 – 160K and 300 – 500K domains. The behavior, coupled with XRD findings, confirm that the devices' contacts are inhomogeneous.

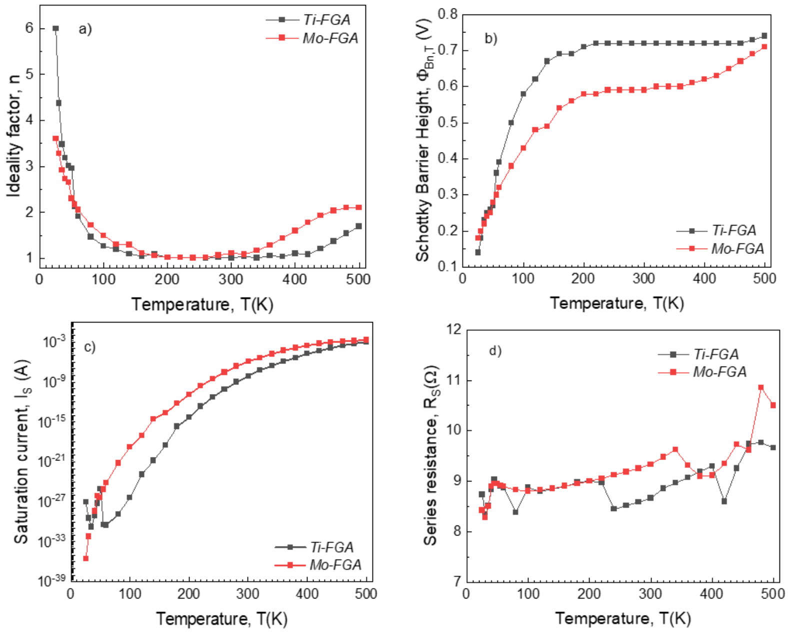

Fig. 4. Temperature variation of electrical parameters for the forming gas annealed Si SBDs.

4.3. Contact-inhomogeneity analysis

Figure 5a) depicts a plot of the nkT product as a function of kT. The green line represents the best case, where n=1. A small deviation from ideality was evidenced for the experimental samples. An usual technique for evaluating such Schottky diodes, with inhomogeneous contacts, is based on the well-known parallel conduction theory [6]. According to it, a practical Schottky contact is made up of several low-area regions (*patches*), each with their own barrier height, set in the nominal interface area (with the desired barrier-height). Werner and Güttler [21] proposed an approach which assumes that the interface presents a Gaussian distribution of barrier heights. They introduced the mean Schottky Barrier Height (Φ_{Bn}^0) and its standard deviation (σ) in order to explain the conventional SBH (Φ_{Bn}^0) temperature dependence as [21]:

$$\Phi_{Bn,T} = \Phi_{Bn}^0 - \frac{q\sigma^2}{2kT}. \quad (3)$$

Both Φ_{Bn}^0 and σ can be determined after representing $\Phi_{Bn,T}$ as a function of q/2kT, from the intercept and slope of the resulting linear trend, respectively. The data taken from Fig. 4b) were used for this plot, yielding results depicted in Fig. 5b).

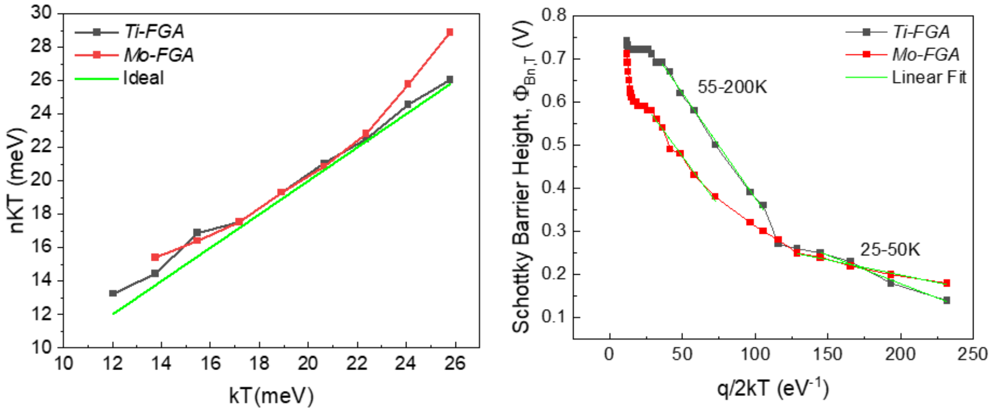

Fig. 5. a) nkT *vs.* kT dependence: deviation from ideality; b) Conventional SBH vs. q/2kT.

However, because of the very large temperatures range, two linear regions were identified, indicating that at least two Gaussian distributions may be present on the contact's surface [22]. One linear region is at very low temperature (25 – 45K) and another one is at temperatures between 55 – 200K. The obtained values for the parameters are listed in Table 1.

Table 1. Extracted values for the mean SBH and standard deviation for different temperature intervals

Extracted parameters						
Temperature range, T(K)	Ti-FGA sample			Mo-FGA sample		
	ΦB^0_{Bn} (V)	σ (V)	σ' (%)	ΦB^0_{Bn} (V)	σ (V)	σ'%
25 – 45	0.44	0.03	6.8	0.33	0.02	6
55 – 200	0.85	0.07	8.2	0.7	0.06	8.5

The mean SBH for the *Ti-FGA* sample is higher by at least 10mV than that of the *Mo-FGA* sample for both temperature ranges. This is explainable by the difference in metal work function values. Table 1 also expresses the standard deviation as a percentage of the mean barrier (σ'), yielding similar values for both samples.

It is worth noting that the parameters obtained in Table 1 are relevant for their respective temperature ranges, but unable to explain the device's overall behavior. This is not surprising, considering that the determination of the mean SBH implies extrapolation at infinite temperature. In other words, Φ^0_{Bn} should express the dominant barrier, governing current conduction, at temperatures approaching the operating limits of the investigated samples. As such, it is clear that the abnormally low Φ^0_{Bn} values obtained for the 25 – 45K range are not valid moving forward. Furthermore, the mean SBH obtained in the 55 – 200K domain, for the *Ti-FGA* diode, is significantly higher than what the trend in Figs. 4b and 5b would suggest. Above 200K, the SBH seems to stabilize at 0.72 V. Conversely, for the *Mo-FGA* sample, the determined Φ^0_{Bn} value within the 55 – 200K range is much lower than what the conventional SBH trend would suggest above 400K (Figs. 4b and 5b).

Moving further, the activation energy (E_a), effective active area (A_{S-eff}) and the mean SBH (Φ^0_{Bn}) were determined from Richardson plots. For this method to be relevant, temperature and bias ranges need to be identified, where the samples have nearly ideal behavior ($n < 1.1$). Analyzing the I-V-T characteristics from Fig. 3 and conventional parameters in Fig. 4, the temperature interval of 160 – 300K was selected for both samples. Considered bias voltages are $V_F(Ti - FGA) = 0.36V$ and $V_F(Mo - FGA) = 0.2V$. The Richardson plots for the two diodes are based on the expression

$$\ln\frac{I_F}{T^2} = \ln(A_S A^*) - \frac{q\Phi^0_{Bn}}{kT}. \tag{4}$$

Re-evaluating the mean SBH requires plotting a modified Richardson curve, according to

$$\ln\left(\frac{I_F}{T^2}\right) - \left(\frac{q^2\sigma^2}{2k^2T^2}\right) = \ln(A_S A^*) - \frac{q\Phi^0_{Bn}}{kT}. \tag{5}$$

The results are illustrated in Fig. 6. The activation energies (0.35eV for *Ti-FGA* and 0.32eV for *Mo-FGA*), obtained from the slopes of Richardson plots (Fig. 6a)) are around three times smaller than the band gap of Si. The effective active area of the Ti-FGA sample, calculated from the intercept, was approx. three times lower than the designed one ($\sim 12.56 \times 10^{-4} cm^2$). For the *Mo-FGA* sample, a value of $0.46 \times 10^{-4} cm^2$ was obtained, almost 27 times smaller. These discrepancies between designed and effective active area indicate that most of the devices' current flows through small, low-barrier patches located on the contact surface.

The mean SBH values, obtained from the slope of the modified Richardson curve (Fig. 6b)), are close to the ones determined from conventional SBH *vs.* q/2kT plots (Fig. 5b)) in the temperature interval of 55 – 200K (Table 1).

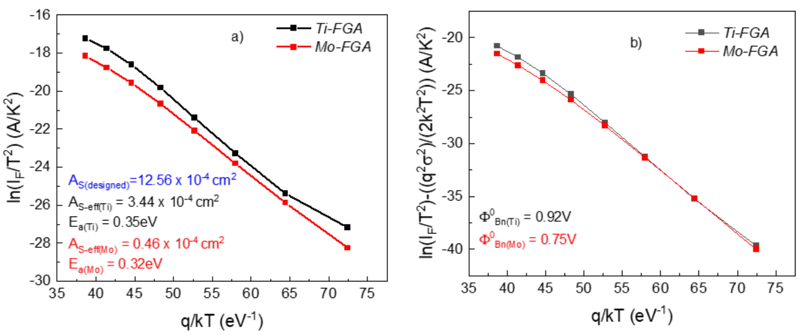

Fig. 6. a) Richardson plot for activation energy and effective active area determination; b) Modified Richardson plot for the mean SBH determination.

The above analysis is obviously useful for confirming the presence of contact inhomogeneity, but is not suitable for determining the parameters that explain the devices' electrical behavior over the entire investigated domain. This is not a major issue in the case of temperatures below 60K, as these cryogenic levels strongly affect device performance, and are outside the scope for most applications. On the other hand, the 200 – 500K interval is of major importance for a large majority of practical situations. Since the investigated samples exhibited irregular variations in both conventional SBH and ideality factor for this range, Werner and Güttler's method could not be reliably used. Under these conditions, a more comprehensive approach is necessary, such as the recently developed *p-diode* model [23].

This model is also based on the parallel conduction concept, with the fundamental distinction that it considers the discrete current contributions of the parasitic regions on the contact surface, rather than lumping them up into a distribution, thus [23]:

$$I_F = \sum_{i=1}^{m} I_{F,i} = \sum_{i=1}^{m} A_n A_S T^2 \exp\left(\frac{-\Phi_{Bn,i}}{V_{th}} - p_{eff,i}\right)\left[\exp\left(\frac{V_F - R_{S,i} I_{F,i}}{nV_{th}}\right) - 1\right]. \quad (6)$$

Each region i is defined by a specific barrier height ($\Phi_{Bn,i}$), series resistance ($R_{S,i}$) and non-uniformity factor ($p_{eff,i}$). The latter one is a parameter that quantifies the degree of inhomogeneity for its associated patch. Large p_{eff} values indicate that the parasitic zones, which dominate current conduction, occupy extremely small areas, meaning that the overwhelming majority of the contact surface is essentially wasted. Thus, the performance of a Schottky diode with inhomogeneous contact can be assessed by analyzing the minimum number of regions *(m)* which are necessary to explain its overall electrical behavior. These regions act as *parallel-diodes*, with varying impact on total current (I_F) depending on temperature and bias domain.

The *Ti-FGA* and *Mo-FGA* samples were parameterized with the *p-diode* technique in the 60 – 500K temperature range. For both samples, $m = 3$ distinct *parallel-diodes* were sufficient to satisfactorily model electrical behavior, as shown in Fig. 7.

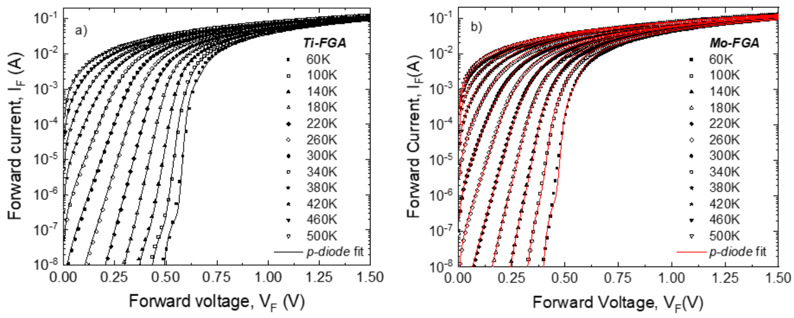

Fig. 7. Measured forward I-V characteristics (symbols) and their *p-diode* fitted counterparts (lines) for a) *Ti-FGA* and b) *Mo-FGA* samples.

Fitted curves were obtained using (6) and the parameters given in Table 2. The value of the ideality factor was kept constant at $n = 1.03$ for all cases. An excellent agreement between measured and calculated data can be observed.

Table 2. *p-diode* parameters for the *Ti-FGA* and *Mo-FGA* Schottky diodes

Parallel-diode	*Ti-FGA* sample			*Mo-FGA* sample		
	Φ_{Bn} (V)	p_{eff}	$R_S(\Omega)$	Φ_{Bn} (V)	p_{eff}	$R_S(\Omega)$
Dp1	0.72	∼0	10.6 – 15	0.6	1.74	12.1 – 16.3
Dp2	0.615	8.05	25 – 50.5	0.54	2.53	40 – 50
Dp3	0.55	10.35	200k – 600k	0.48	6.44	∼50k

For the *Ti-FGA* sample, in the 140 – 500K temperature range and 1μA – 100mA current interval, a single dominant contact region (Dp1) is predominantly responsible for current flow.

This zone corresponds to the nominal Schottky contact, covering roughly the entire area (deduced from $p_{eff} \cong 0$). Its associated barrier height is also in agreement with values extracted for $\Phi_{Bn,T}$ above 200K in Fig. 4b), proving the relevance of this model for practical diode performance evaluation. In order to explain the inhomogeneous behavior of the electrical characteristics below 180K, it was necessary to consider two additional low-barrier contact regions (Dp2 and Dp3) in the *p-diode* model ($m = 3$) [23]. Their high p_{eff} values (Table 2) suggest that Dp2 and Dp3 occupy areas much smaller than the overall Schottky contact surface (under 0.05% of the nominal value). Dp3 influences current conduction only at low current levels, under 180K, motivating its very large associated R_S values. It is concluded that the *Ti-FGA* diode has an overall good contact quality and is suitable for applications especially above 140K and over 1μA bias.

On the other hand, for *Mo-FGA* there are two regions (Dp1 and Dp2) with significant influence over total current across the entire temperature domain. Dp1, similarly to the case of *Ti-FGA*, has barrier values close to those in Fig. 4b) above 200K, occupies roughly 17.5% of the contact area and is responsible for currents above 100μA. Dp2, with a lower SBH, covers approx. 8% of the surface and has dominant influence between 1μA and 100μA. Once again, Dp3, with the highest series resistance, has a significant conduction impact under 1μA. Consequently, this sample has a more pronounced degree of contact inhomogeneity, which restricts the domains where it operates reliably.

Thus, an in-depth characterization methodology was applied for the experimental Schottky barrier diodes, which was able to fully explain forward electrical behavior in a comprehensive range of temperatures, even exceeding normal operation limits.

5. Conclusions

This paper presented a thorough characterization of silicon Schottky diodes with Ti and Mo contact metallization. Experimental samples were subjected to thermal treatment in forming gas in order to obtain a more uniform metal/semiconductor interface. The annealing process yielded improvements in terms of electrical behavior, as demonstrated by current-voltage characteristics over a wide temperature interval (15 – 500K). Even so, an XRD analysis evinced that there were multiple metal silicide compounds present on the contact area. The inhomogeneity was also confirmed by the results of conventional parameter extraction for the Ti and Mo samples. Both diodes exhibited Schottky barrier height and ideality factor variations with temperature.

Werner and Güttler's inhomogeneity model was used in order to explain the samples' electrical behavior, indicating the presence of at least two Gaussian distributions of barriers on the contact surface. Because of the very wide range of investigated temperatures, this approach could only be used for the 25 – 200K interval. The two sets of parameters (mean barrier height and dispersion), obtained for 25 – 45K and 50 – 200K, respectively, had no relevance for diode behavior at higher temperatures.

Our *p-diode* technique was also used to assess the devices' behavior. According to it, each experimental sample could be fully modeled as three ideal diodes connected in parallel. Model-fitted curves were in excellent agreement with measured data over a 60 – 500K temperature range. The associated parameters of these *parallel-diodes* quantitatively evaluated the performance of the overall devices.

For the *Ti-FGA* diode, a dominant SBH of 0.72V was determined, associated to nearly the entire contact area. At low bias and temperature, two additional zones, covering less than 0.05% of the total surface, also contributed significantly to current conduction. This analysis determined that the sample is suitable for applications over a sizeable bias and temperature domain.

Conversely, two regions, occupying 17.5% and 8% of the contact area, were mainly responsible for conduction in the *Mo-FGA* diode at all temperatures. The associated barrier heights were 0.6V and 0.54V, respectively. One additional zone, with a SBH of 0.48V and area under 0.25% of the nominal one, was influential at low currents, under 1μA. Thus, this sample exhibited restricted intervals where its behavior was suitable for applications.

While the *p-diode* model could be applied even under 60K, there are two drawbacks. First, the number of *parallel-diodes* required for modeling would increase, which leads to higher data processing and parameter extraction times, and only serves to confirm the deterioration of device behavior under 60K. Secondly, at such cryogenic levels, mechanisms other than thermionic emission account for current value, such as carrier freeze-out, which diminish the physical significance of extracted parameters. This was proven when trying to use the Gaussian distribution approach for the 25 – 45K domain. The resulting mean SBH of 0.32V is unfeasibly low for a Schottky diode.

Overall, the paper demonstrates that a comprehensive characterization approach needs to be undertaken in order to fully explain Schottky diode electrical behavior over wide temperature ranges.

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