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Design, Fabrication and Characterization of 10 kV 4H-SiC BJT for the Phototransistor Target

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Abstract. For medium voltage, the SiC BJT is a convenient solution to reduce the on-losses and it could have the advantage to be optical controlled, to ease the serial connection of BJT. The design of a 10 kV, 10 A SiC BJT is described. The different fabrication steps are described. The analysis and optimization of the peripheral protection are described in detail. The fabricated wafers consist in several types of electrical BJT and diodes. Moreover some phototransistors have been fabricated. The selected solution is a combination of a JTE (*Junction Termination Extension*) and guard rings. The first measurement results are present. Some vacuum chamber probe level measurements have shown breakdown voltage up to 11 kV. Probe measurements of the forward characteristic have shown a good operation of the electrical BJT, with a current gain up to 20. Some dies have been packaged to achieve high-current measurement. The on-state characterizations show on current up to 15 A with a current gain that reach 15. First optical control tests have shown encouraging results.

Key-words: Bipolar junction transistor; high-voltage power semiconductor device; peripheral protection; power electronics; silicon carbide.

1. Introduction and Preliminary Results

Ecological transition [1] is a public policy applied explicitly or implicitly in most of the world countries. It implies the sustainable development and the target to reduce the greenhouse emissions with a clear target to increase electrification to reach such an objective. *Silicon Carbide* (SiC) is one of the new semiconductor materials that benefits of such a target for instance for the electric vehicle technologies. In 2022, the SiC power semiconductor market reaches USD 1 billion and is supposed to attain USD 15 billion by 2032 [2]. However, the availability of such new power semiconductor devices with very good properties, enable to develop numerous other studies for new applications of such devices. For instance, one can already considered photovoltaic (PV) inverters, electric traction as railway applications and even other stationary applications (wind power, data centers, industry) [3]. An I–V curve comparison is illustrated in Fig. 1.

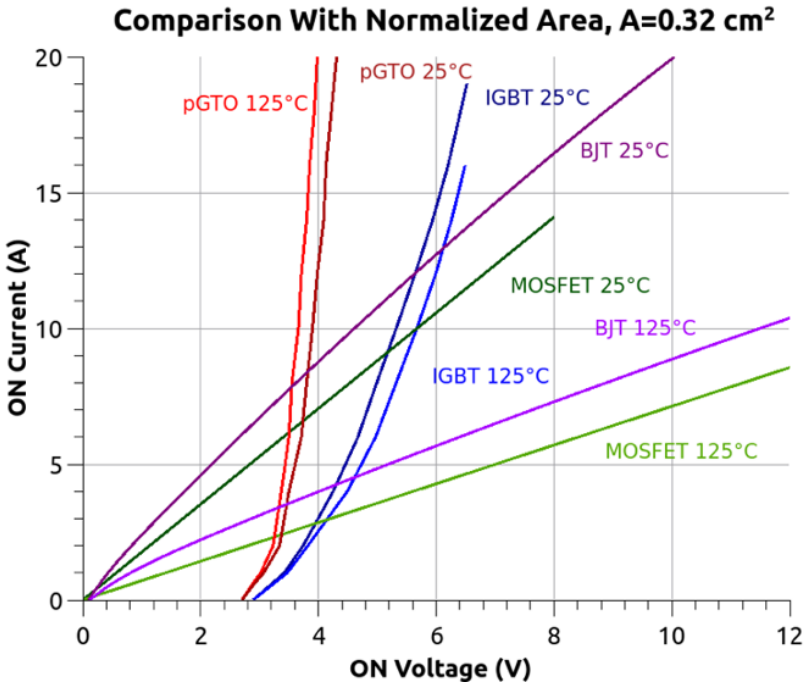

Fig. 1. I–V curve comparison of 15 kV SiC P-GTO, IGBT and MOSFET at 25 °C and 125 °C [3] and authors' fabricated device 10 kV BJT (for $I_B = 1A$).

In comparison to Si-based component, for the same level of conduction losses, SiC power components, enables a clear reduction of the switching losses [4]. That enables a possible reduction of total losses or for embedded applications a clear reduction of the size and mass of the converters.

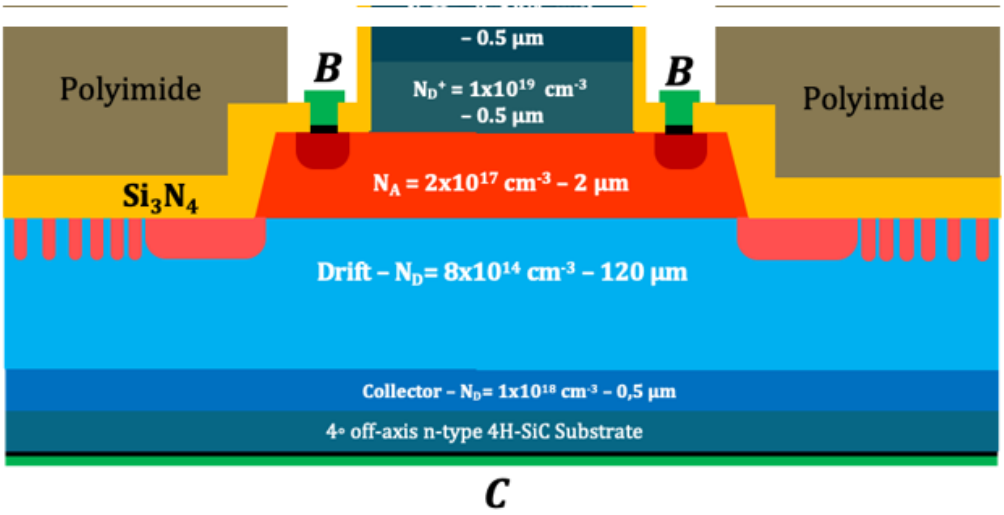

Fig. 2. Schematic cross-sectional view of 4H-SiC NPN BJT, with detailed epitaxial layers (thickness and doping level).

Concerning high-voltage devices, bipolar devices such as thyristors, GTOs, BJTs and IGBTs potentially enable a reduced drop voltage with respect to unipolar devices as shown in the cross-sectional view of the Bipolar Junction Transistor in Fig. 2 [4].

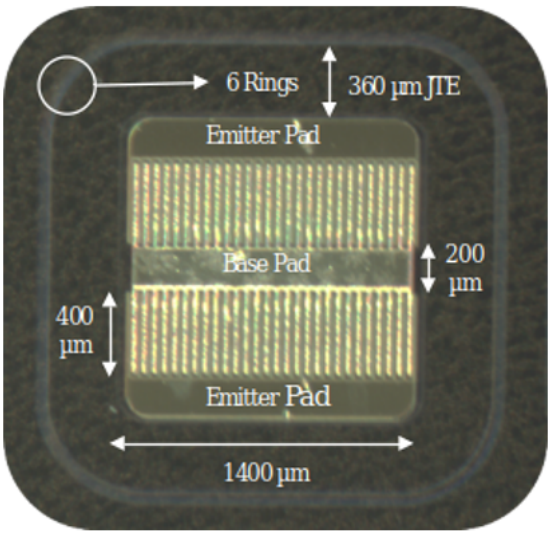

Fig. 3. Top microscopic view of 0.053 cm^2 fabricated BJT device with 2 emitter pads.

The blocking voltage could be very high as 27 kV for a SiC IGBT [5] but the cost of fabrication of such a device is too high for commercialization. However, power SiC modules 3.3 kV,

750 A are available [6] with the target of railway applications [7].

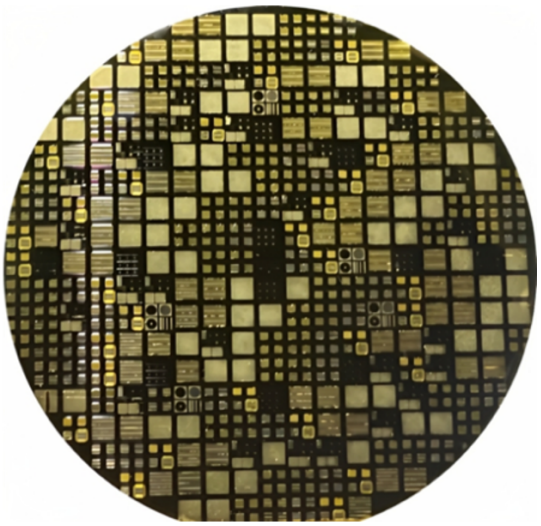

Fig. 4. Picture of the top view of a fabricated wafer.

Another advantage of bipolar power devices is the capability to be optically driven [8] which could simplify the serial association for high-voltage applications. This was the main motivation for the project that supports this paper.

High-voltage bipolar devices such as BJTs based on 4H-SiC are considered very attractive candidates for high-voltage applications. In particular, when compared to silicon thanks to a high breakdown electric field resulting in decreasing the on-resistance and probably avoiding a second breakdown avalanche effect [9]. In addition, a high saturation velocity and reduced device areas enable fast switching and its wide-band gap that allows it to operate over high temperatures [10].

Finally, a good thermal conductivity gives it the ability to easily transfer the heat generated by Joule's effect to a heat sink [11]. The recent literature reported high voltage 4H-SiC BJTs include a 10 kV open-base breakdown voltage (BV_{CEO}) and a specific on-resistance of 130 mΩ.cm^2 at (RT) with a 120 μm drift layer doped to 6×10^{14} cm^{-3} [12]. A 15 kV (BV_{CEO}) at a leakage current of 0.1 mA/cm^2 with 125 μm drift layer doped to 1.1×10^{14} cm^{-3} [13]. And a 9.2 kV (BV_{CEO}) with a 50 μm, a 7×10^{14} cm^{-3} doped drift layer and $R_{SP\_ON} = 78$ mΩ.cm^2 [14].

For high-voltage applications, it is mandatory to implant a highly sophisticated base-drift *junction termination extension* (JTE), which serves in minimizing the electric field plate crowd generated at the MESA edge of the power device. Several approaches were applied to optimize the extension performance such that applying variations over the length and etching depth of the JTE [13], or by implanting different doses over the total length of the JTE [15], and by the addition of extra implanted rings [16]. In this paper a more than 10 kV NPN BJT based on 4H-SiC is reported when the theoretical value determined by its drift layer thickness and doping concentration is almost 13 kV.

Both the device design using TCAD (Sentaurus Synopsys) [20] for the peripheral protection and fabrication process are more detailed in Section 2. The electrical characterization of the fabricated device is shown in Section 3. The extended current capability is evidenced.

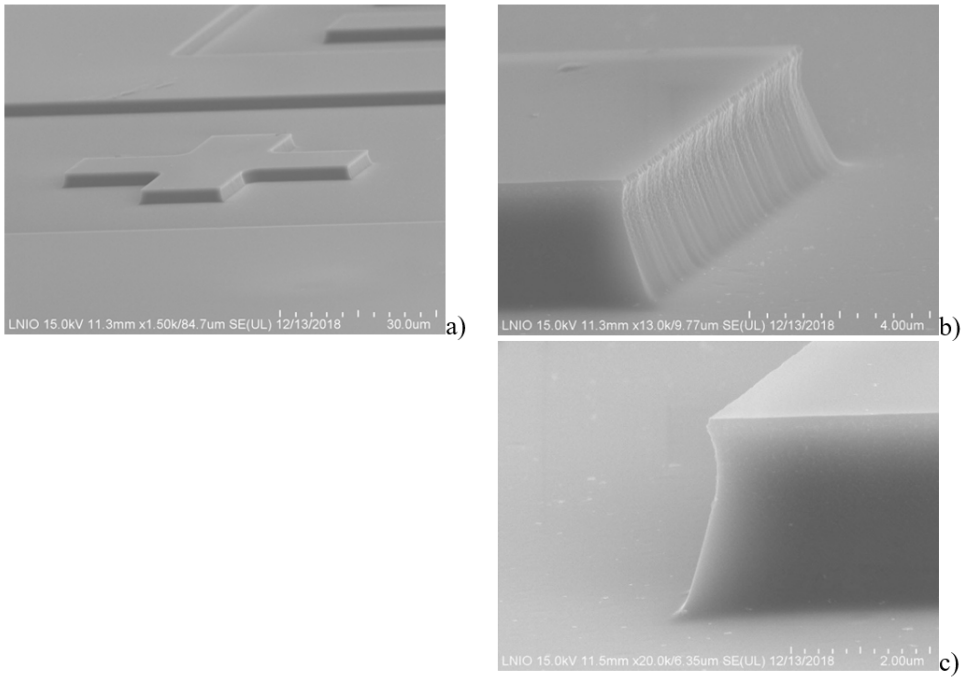

Fig. 5. Test motif for etching(a), quasi-vertical trenches (b), corner trench (c).

2. Device Design and Fabrication

Fig. 2 represents a typical cross-sectional view of authors' fabricated BJT with five epitaxial layers grown on a ~ 300 μm 4° off-axis 4H-SiC substrate. Fig. 3 shows a top view of a fabricated BJT device with 2 emitter pads and Fig. 4 an image of 100 mm processed 4H-SiC wafer. To avoid equipotential line tightening and high electric field peaks in this area under reverse bias at high-voltage, rounded corners with radius of 120 μm and 250 μm have been chosen at the periphery.

Eleven photolithographic levels have been processed during the fabrication of the NPN BJT.

The first two levels concern a 1.2 μm and respectively 2.2 μm deep plasma etching of the 0.5 μm n-type emitter doped to 10^{19} cm^{-3} meeting another 0.5 μm emitter highly doped to 3×10^{19} cm^{-3} and a 2 μm p-type base doped to in SF_6 chemistry with an ICP/RIE (Inductively Coupled Plasma Reactive Ion Etching) Plassys MU400 reactor.

The process has been optimized with high ICP density plasma (1000 W) and high RIE bias (~ 350 V) to obtain quasi-vertical trenches (Fig. 5(a) and Fig. 5 (b) with rounded sides walls at the bottom part, to avoid trenching phenomenon [16], as shown in Fig. 5 (c).

To avoid equipotential line tightening and high electric field peaks in this area, under reverse bias at high-voltage, the round angle of the peripheral has been select among two different values: 120 μm and 250 μm (Fig. 12).

After plasma etching two doping steps with Al ion implantation steps have been performed, in the p-type base to ensure a low resistive ohmic contact and to implant the peripheral protection. To avoid SiC amorphization the high-doped base wells have been implanted at 300°C.

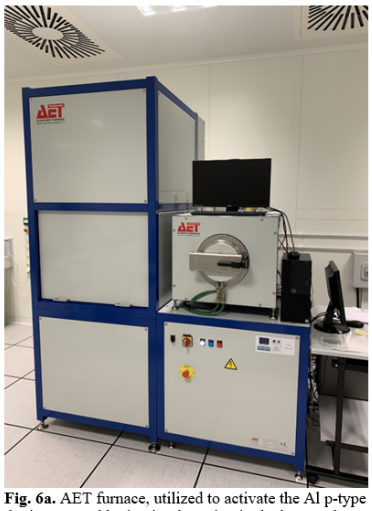

Fig. 6a. AET furnace, utilized to activate the Al p-type doping created by ion implantation in the base and periphery (a).

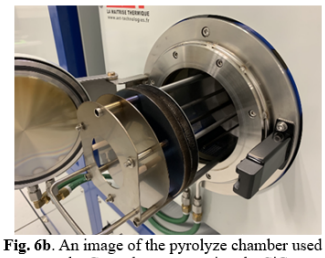

Fig. 6b. An image of the pyrolyze chamber used to create the C-cap layer protecting the SiC during high temperature annealing (b).

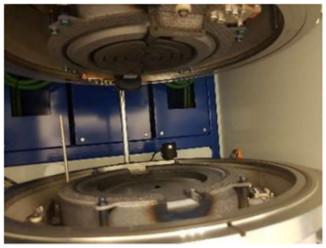

Fig. 6c. The RTP chamber with double graphite resistors utilized to perform the doping activation annealing at 1700°C (c).

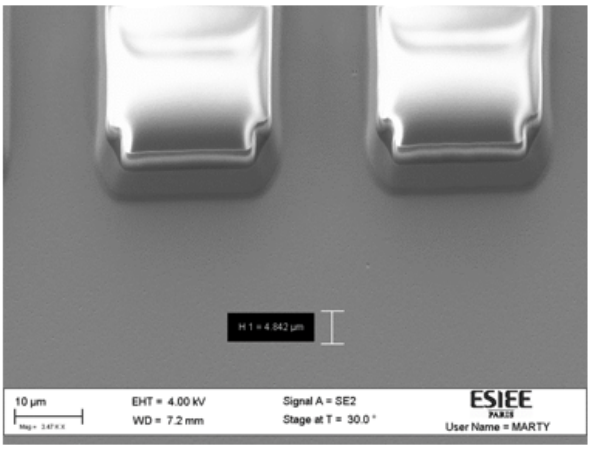

Fig. 7. An image during the technological process with the BJT defined fingers.

To activate dopants, post-implantation annealing has been performed with a 1700°C/30 min plateau in an AET 6" RTP furnace with graphite resistors, specially designed for this process (Fig. 6 (a), (Fig. 6 (b) and (Fig. 6 (c)). Previously the samples have been encapsulated on both sides with a C-cap obtained by pyrolyzing AZ photoresist. The C-cap has been after being removed by O_2 plasma. The lowly n-doped drift layer has a thickness of 120 μm and a doping concentration 8×10^{14} cm^{-3}.

The next technological steps concerned the materialization with ohmic contacts formed on the high p-doped and n-doped (on both sides) layers. For the n-type emitter and collector, sputtered Ni layers were patterned, and RTA annealed at 900°C, and an alloy of Ni/Ti/Al 800°C RTA annealed [17] for the p-type base contacts.

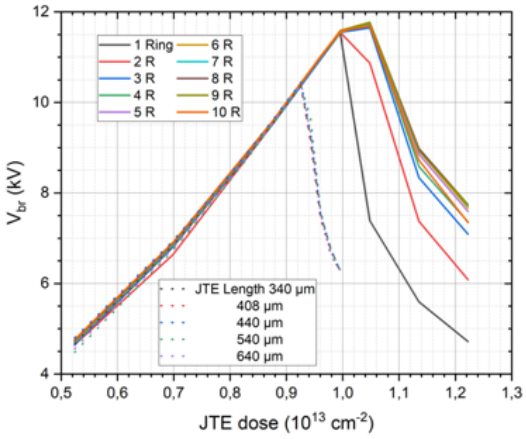

Fig. 8. TCAD simulation of the variation of Blocking Voltage (kV) as a function of JTE implanted Dose and JTE Length.

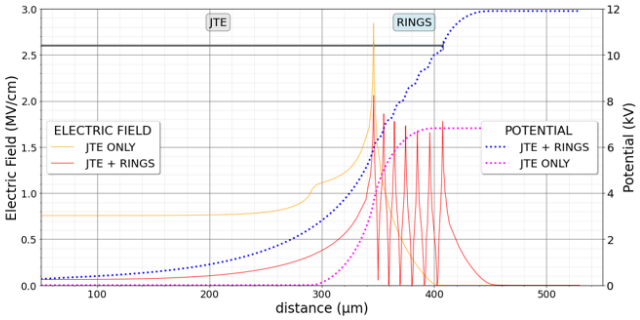

Fig. 9. Electric field and potential distribution over the horizontal axis through the peripheral protection as shown in Fig. 14.

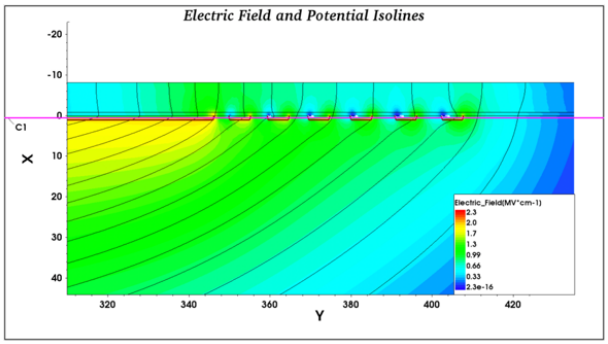

Fig. 10. TCAD simulated Electric Field and Isopotential Lines (600V steps) around the 6 rings for JTE+RING optimal design and magenta cross section for Fig. 9 and Fig. 11.

For assuring a uniform potential distribution along metallized fingers, gold over-metallization has been performed by sputtering and patterning (Fig. 7).

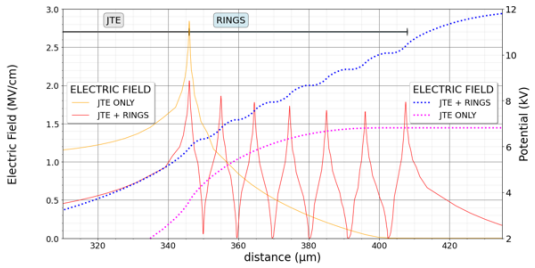

Fig. 11. Electric field and potential distribution over the horizontal axis cross section showing the uniform potential smoothing and optimal termination (Electric Field: red, Potential: blue) design and benefits against JTE only (Electric Field: orange, Potential: magenta).

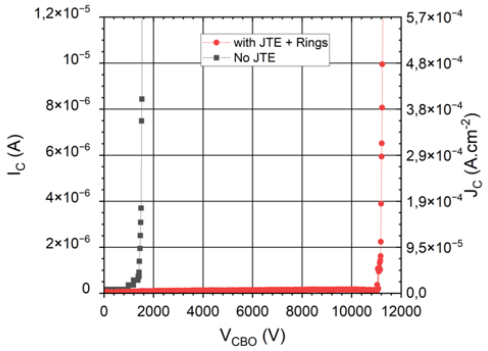

Fig. 12. Reverse IV characteristics recording an open emitter blocking voltage of 11 kV at room temperature w and w/o JTE. The recorded results belong to the device shown in Fig. 14.

Before the metallization steps SiC wafers have been thermally oxidized with a combined wet/dry process and the different metallic layers were isolated with LPCVD and PECVD Si_3N_4 layers locally opened by SF_6 plasma RIE. At the end, a last passivation layer has been patterned on the surface with a thick polyimide of 12 μm.

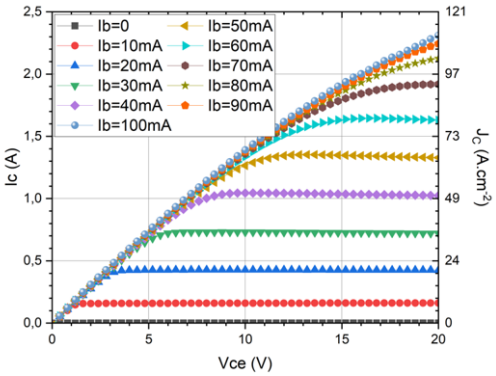

Fig. 13. Forward I-V characteristics of the fabricated BJT with an active area of 2.06 mm^2 measured on a probe station.

The peripheral protection is made of a 360 μm long JTE (Junction Termination Extension), done by Al implantation with an optimum dose of 1.1×10^{13} cm^{-2} determined by TCAD simulations [19] (Fig. 8). Lengthier JTE won't provide any benefits. The peripheral protection is then completed by a set of several rings, each 5 μm long, with a 4 μm spacing between the JTE and the first ring. After that, a space increase of 0.5 μm is given between each ring, each time a ring is added (*i.e.* the space between 1st and 2nd ring is 4.5 μm, between 2nd and 3rd is 5 μm). The TCAD simulations show that the addition of one supplementary ring will push further the maximum expected breakdown voltage while shifting the optimum dose to higher values. Therefore, by keeping the JTE dose at 1.1×10^{13} cm^{-2}, the breakdown voltage is becoming less sensitive to process variation as it will less likely be located on the right-hand side of the sharply decreasing curve.

Fig. 9 and Fig. 10 show the simulated electric field profile of the fabricated device whose the ring number is set to 6. This value was chosen as the gain in holding voltage capability becomes less pronounced for higher ring numbers. The peripheral protection design and parameters such as JTE length, ring number, and implanted dose were extracted from [18] upon a study done on a simulation model using TCAD from Synopsys Sentaurus [20] by performing various breakdown simulations to detect optimum technological parameters. The electric field distribution shown in (Fig. 11) shows the impact of having such an optimized system to ensure a smooth flow of the high electric field that accumulates at the junction termination, increasing by this phenomenon the blocking voltage.

3. Results

Electrical characterizations were performed on the fabricated devices. Reverse IV characteristics as shown in Fig. 12 were performed using a high vacuum probe station at ISL [21]. A high-blocking voltage of 11 kV with a leakage current density of 0.1 mA/cm^2 was recorded, validating authors' model and simulation results.

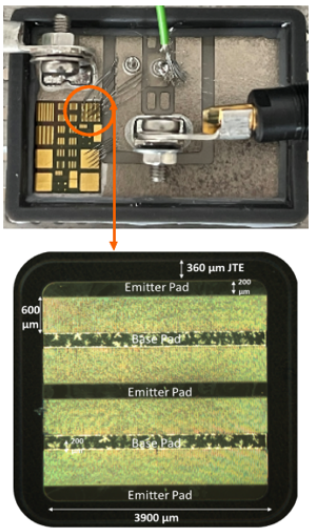

Fig. 14. Top: picture of a package with several dies to achieve high-current measurements. Bottom: picture of the bounded BJT die.

The efficiency of authors' peripheral protection can be clearly visualized when comparing both graphs in Fig. 9 and Fig. 11 the distribution of the electric field all over the device due to the junction termination extension (red curve in Fig. 9) when compared to the electric field in the absence of a rings (orange curve) lead to a great increase in blocking the voltage from 7 kV without rings to 11.8 kV with a well-parameterized JTE + RINGS. Fig. 10 shows a uniform potential distribution in both SiC material and passivation layers on top of the semiconductor. The TCAD simulations results have been confirmed with breakdown voltage measurements. The blocking voltage increases from 1.3 kV when the JTE is absent (Fig. 12) to 11 kV with a well-parameterized structure.

Fig. 13 shows forward common-emitter current-voltage I-V characteristics at room temperature, of the fabricated BJT (Fig. 14) with an active area of 2.06 mm^2 and an emitter finger width of 25 μm long. The maximum current gain achieved is $\beta = 27$ at a base current $I_B = 70$ mA and $V_{CE} = 20$ V for a collector current of $I_C = 1.9$ A (Hexagonal Symbol), corresponding to a current density of 92 A/cm^2.

To achieve high current measurements, some dies were packaged as shown in Fig. 14, and the on-state characteristic is illustrated in Fig. 15. This new packaging has been improved since authors' previous paper on this topic [19] presented in CAS conference. If the current gain is a little reduced with respect to probe measurements shown in Fig. 16, the current gain reduction from 20 to 15 seems due to the change of emitter fingers, as shown just below.

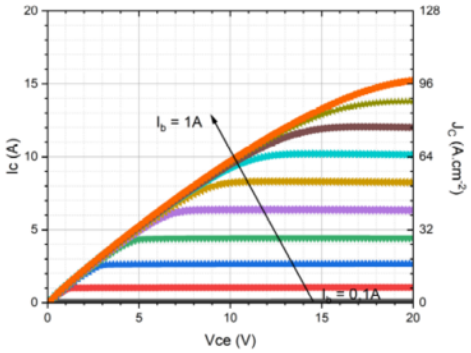

Fig. 15. On-state characteristic of the 5 mm × 5 mm electrical BJT shown in Fig. 12. The current gain reaches 15.

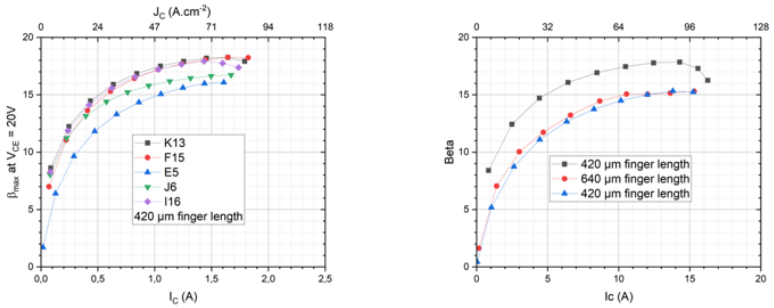

Fig. 16. Analysis of the current gain for various finger length of large electrical BJTs (5 mm × 5 mm) (a), analysis of the current gain for various small electrical BJT designs (1.4 mm × 1.4 mm) (b).

4. Conclusion

In this article, a more than 10 kV class BJT based on 4H-SiC is reported with an optimized junction termination extension and an isolation ring system. The fabricated device attained 11 kV as open base breakdown voltage, which corresponds to almost 90% of its theoretical value, at a leakage current of 10 μA. The raw dies also show at room temperature a maximum current gain $\beta = 27$ at a base current of 70 mA, current density of 92 A/cm^2 and a total collector current of 1.9 A. The packaged dies show higher current level 15 A with a little reduce current gain, about 15. A second lot of fabrication is under progress and a higher number of dies with a breakdown voltage greater than 10 kV is expected. Hard switching measurements are also planned up to 7 kV applied voltage and 20 A switched current. The next target will be to characterize optical controlled BJTs, which have been designed in the same project.

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