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SiC Plasma and Electrochemical Etching for Integrated Technology Processes

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Abstract. This paper reports research on deep etching of *silicon carbide* (SiC) to achieve isolated deep trenches in the same thick SiC substrates. This paper combines both plasma etching and electrochemical etching on p-type SiC above n-type SiC layers. Uniform and smooth plasma etched surfaces of SiC were obtained upon using Ni masks with significant thicknesses deposed by electroplating. This step allowed to etch unprotected SiC up to 30 μm. Selective conductive electrochemical etching allows to obtain a higher etched thickness of silicon carbide substrates. The p-type layer will be inert and act as a stop layer, whereas, the n-type layer will be corroded. Finally, this paper obtains deep etching reaching around 80 micrometers, which opens the perspectives to start fabrication of vertical power-integrated SiC devices.

Key-words: APTES; etching; ICP; Ni electroplating; plasma; RIE; SiC.

1. Introduction

Silicon carbide has been classified as one of the hardest materials in the world. The strong hardness of *silicon carbide* (SiC) involves a difficult technology in the manufacture of semiconductor devices but which has nevertheless reached a certain maturity today in power electronics. Compared to more classic silicon, thanks to its larger bandgap and capability to support high electric fields, SiC power devices are superior to silicon in terms of high temperature operation, fast and high voltage performance.

The reliability in power electronics is also improved by using SiC, and integrating several power devices in the same SiC chip is expected to enhance the switching operation speed and decrease the power loses. To fabricate integrated power circuits, new technologies developments

are required in the fabrication of SiC microelectronic systems. One of the technological critical point to integrate several power devices in the same SiC chip is to realize deep etching thickness, in order to insulate them. And in the case of an integration of vertical devices, etching via through the entire SiC substrate (several hundred of μm) are necessary.

Classical plasma etching of only a few micrometers of silicon carbide is already solved and reported in previous studies [1–4]. In this case the use of Ni as a mask during SiC plasma etching has been found to reduce the micromasking effect, in addition to its good selectivity for SiC up to $\sim 50:1$ in SF_6/O_2 *reactive ion etching* (RIE) plasma compared to other hard masks (as metals), such as aluminum. Consuming the Ni mask during RIE and/or *inductive coupled plasma* (ICP) etching could be a rate-limiting step in SiC etching. To increase the etching depth, high-thickness Ni layers are needed, which are difficult to produce by classic *physical vapor deposition* (PVD) methods, such as evaporation or sputtering. The originality of our previous work showed a high adhesive layer of electroplated Ni metal layer on the SiC substrate allowing for duplicating the plasma etching, without consuming the Ni metal mask [5]. This adhesive metal layer has been stabilized through growing palladium nanoparticles on the thin silicon oxide layer natively presented on the silicon carbide substrate.

We obtained a considerable etched thickness of SiC up to 30 μm using an ICP/RIE optimized process. Then, in order to increase the etching depth in SiC beyond the plasma etching limits, we compare the performed plasma etching with an electrochemical etching. Based on the reported studies by Shor et al. [6], this paper performs electrochemical etching and obtains an etching thickness superior to 80 μm.

This paper compares the etching thickness and surface morphology of the SiC obtained using plasma etching, with the etching thickness and surface morphology of the SiC obtained using electrochemical etching. In the first part, it is shown that the results obtained with the plasma etching using high adhesive Ni metal layer as a mask on the SiC substrate. In the second part, this paper describes the electrochemical etching process using p-type SiC as an inert layer.

2. Experimental Part

Commercial n-type silicon carbide, 4H-SiC, 4° off-axis substrates have been utilized for this study on Si-face.

2.1. *3-Aminopropyl triethoxysilane* (APTES), functionalization step, growth of Pd nanoparticles and Ni electroplating

3-Aminopropyl triethoxysilane (APTES), was attached on the SiO_2 thin layer natively present on the SiC surface, through the hydroxyl group formed with O_2 plasma treatment. This method was investigated previously in order to adsorb APTES on oxidized aluminum [7]. 1mL of APTES was dispersed in 20 mL of a toluene solution. The SiC substrates were immersed in prepared toluene solution containing silane precursor for 24 hours. The resulting amino silane functionalized SiC surface were finally washed with toluene, air dried, and kept in glove box for the next step.

The amine functional group on the other edge is now free to participate in further surface modification reactions (Fig. 1 A).

The activation of the substrate covered with APTES was performed by immersion into an aqueous solution that contained 0.5 g/L of $PdCl_2$ and 20 mL of 37% HCl at room temperature (RT) for 10 min.

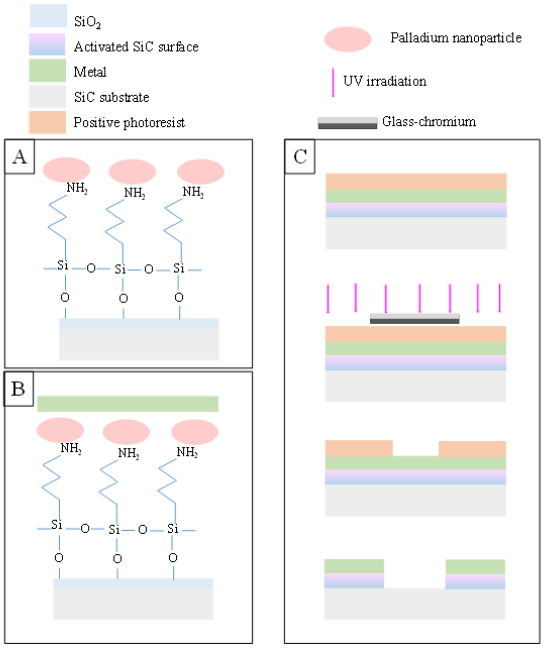

Fig. 1. A) APTES functionalized SiC substrate. B) Ni electroplated on a functionalized SiC substrate. C) Photoresist deposition on the Ni layer, photolithography, and wet etching to obtain the target pattern.

The electroplating solution consists of 1750 mg of (Ni $(NO_3)_2 6H_2O$), 1500 mg of ($NiSO_4.6H_2O$) with 2600 mg of boric acid in 500 mL water. The activated samples were coated via an autocatalytic reaction forming a metallic layer deposited from the dissolved Ni ions in the solution at RT for 2 min with an applied current of 0.05 A (Fig. 2).

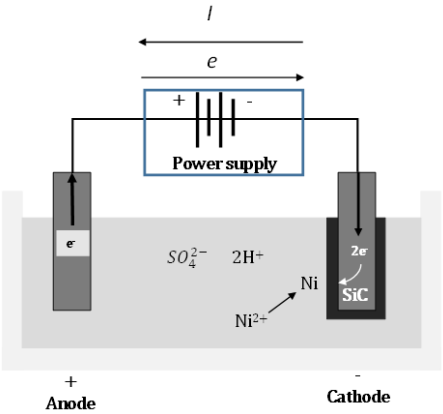

Fig. 2. Schematized image of nickel electroplating on silicon carbide substrate.

2.2. Ni mask pattering and SiC etching

To pattern the Ni layer mask, the seemingly simple process of spin coating accomplishes a thick and uniform coating of AZ9260 positive photoresist (Fig. 1 C).

After coating, the resist film was annealed at 115°C for 15 min. UV photo exposure was done using optical lithography photomask alignment machine (SUSS MicroTec MJB4), for 75 seconds at hard contact with a glass chrome mask. Post-exposure: the substrate is dipped within AZ 726MIF developer. The uncovered metal area was etched using a mixed of orthophosphoric, nitric and acetic acid solution, by dipping the substrate at 60°C for 2 hours, and then the photoresist removed with acetone.

Silicon thin layers are also deposited on the Ni layers to increase the volatility of the Ni by-products, avoiding thus micromasking during SiC plasma etching process [4]. The deposition of silicon was done by electron-beam gun evaporation with Plassys MEB400 machine, at low pressure of 1.6×10^{-6} mbar.

The patterned SiC substrates were etched using ICP/RIE Plassys MU400 reactor. The utilized reactor is composed of two power sources: RIE to form the plasma potential at the substrate surface and ICP to enhance the density of reactive species. The etching gases used are SF_6 and O_2. Fluorite ions strike the SiC surface and dissociate the Si-C bond, creating SiF_x and CF_x volatile species. Oxygen atoms enhance the fluorine atoms generation and interact with the carbon layer creating also volatile CO_x species.

2.3. SEM characterization

The morphology, the patterned masks and the etched trenches were studied using optical microscope (Nikon eclipse) and by field emission scanning electron microscopy (SEMFEG) with Hitachi SU8030 equipment.

3. Results and Discussion

3.1. Surface activation

APTES treatment was applied on SiC substrate to graft silane with the hydroxyl group formed through O_2 plasma treatment on the native silicon oxide layer on the surface. The APTES easily reacted with the hydroxyl group forming a *self-assembled monolayer* (SAM) of organic molecules.

The binding mechanism of Pd (II) to the amine-terminated SAM was already applied by Guo *et al.* [8] on polyester. We followed the same procedure to create Pd colloids on the SiC surface as active catalyzers for Ni electroplating. The Ni coating is formed from the dissolved Ni ions in the solution (Fig. 3).

We applied Ni electroplating successfully, directly on the SiC without adding APTES/ Pd catalyzers. Nevertheless, we realized that the metal is not stable on the bare SiC surface compared to the functionalized substrate as shown in Fig. 4. Crakes can be observed clearly on the SiC surface compared to Fig. 3, where the metal layers appear denser.

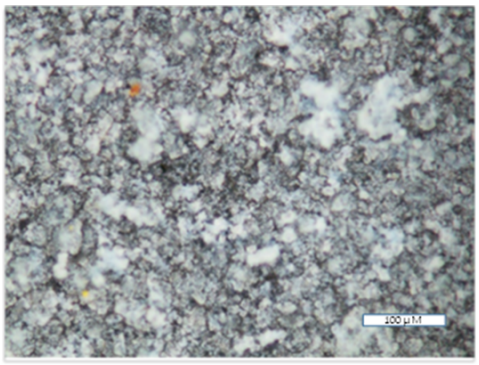

Fig. 3. Optical image of Ni electroplated on a Pd activated SiC substrate.

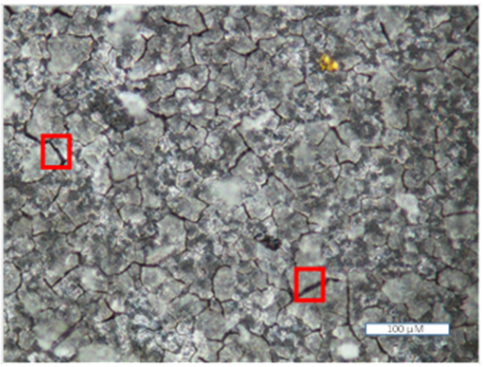

Fig. 4. Optical image of Ni electroplated directly on SiC substrate.

3.2. Kinetic etching and surface morphology

Following Ni deposition on the surface of SiC substrate, the desired Ni pattern has been obtained using ~ 12 μm AZ9260 photoresist, through defining the uncovered metal area needed to etch SiC as shown in Fig. 1 C.

The etching parameters used in our ICP/RIE plasma reactor are composed of 8 mTorr work pressure, 25 sccm SF_6 and 7 sccm O_2 gas flow, 1000W ICP power and 180W RIE power (430V bias). These parameters were adapted to our ICP/RIE reactor from our previous studies done on RIE reactors [1–4].

Fig. 5 A and B correspond to an etched SiC surface before and after metal removal. Fig. 5 B shows an average etching depth of 12 μm obtained after 30 min etching and thus with a 0.4 μm/min etch rate. The jagged profiles at the SiC etched trenches come from the lithography process of our positive resist which has an unusual high thickness but necessary to well delimit the Ni formed electroplating layer.

The thickness of the Ni deposited on the SiC surface remained with approximately the same size, ~ 3 μm, after SiC etching. These results allow us to perform more plasma etching steps to obtain higher etching thickness. A new step of Si e-beam evaporation has also been added before a new plasma etching in order to avoid micromasking [4].

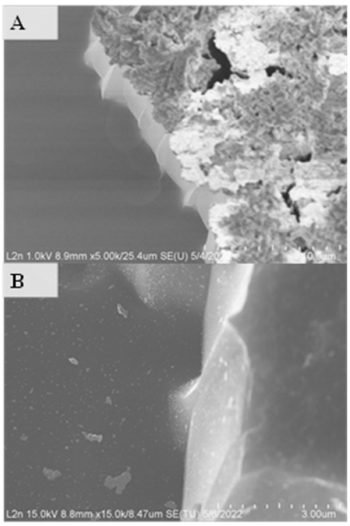

Fig. 5. *Scanning electron microscopy* (SEM) images of SiC substrate etched with Ni electroplated masks before (A) and after (B) removing the Ni electroplated metal layer.

Fig. 6 shows a DEKTAK Bruker stylus profile on SiC substrate, ICP/ RIE plasma etched 2 times (30 min each) resulting in a ~ 3 μm etched thickness after Ni mask wet removed.

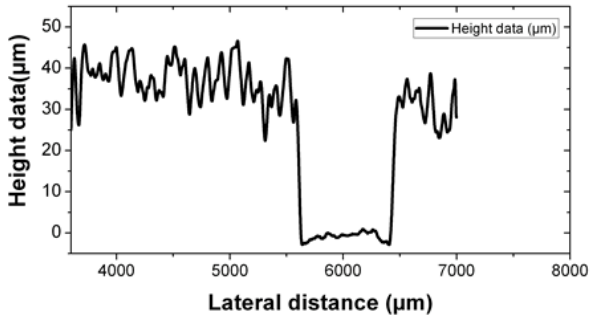

Fig. 6. Film thickness profile measurements for Ni patterned Pd activated SiC substrate after two steps ICP/ RIE etching.

Fluorinated plasma of SiC patterned by electroplated Ni mask resulted by an etching thickness up to 30 μm. To insulate vertical power devices within the same SiC substrate we need more than 100 μm of etching thickness. Electrochemical etching was already employed to achieve deep etching thickness in SiC [9]. A selective conductivity etching of a SiC with an etch-stopping layer corresponding to p-type SiC can occur at open circuit potential due to the energy band bending difference of the n-type and p-type SiC in the KOH electrolyte solution [6].

We patterned (by fluorinated plasma) p-type SiC on the surface of n-type SiC as a sacrificial layer and stop layer (Fig. 7) to perform electrochemical etching in the n-type substrate. We obtain an etching thickness in the substrate, down to 80 μm as shown in the DEKTAK Bruker stylus measurements in Fig. 8.

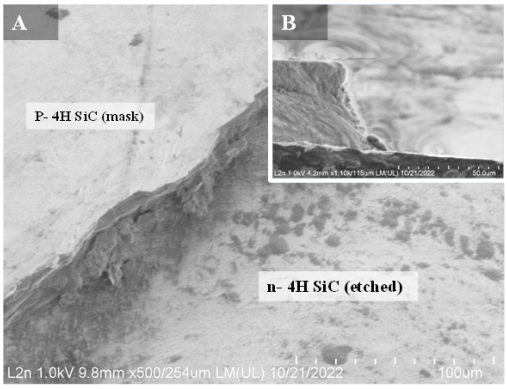

Fig. 7. A) SEM images of SiC n-type etched surface (to the right) using p-type SiC layers as a mask. The B) inset showed the vertical etched trench.

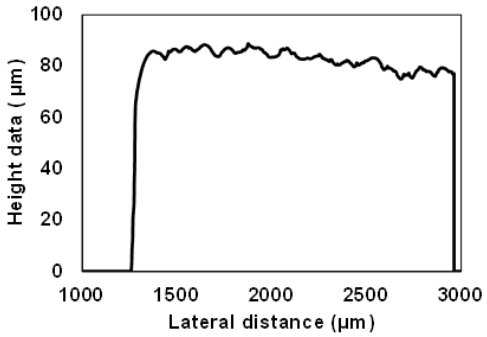

Fig. 8. Film thickness profile measurements for the electrochemical etched SiC.

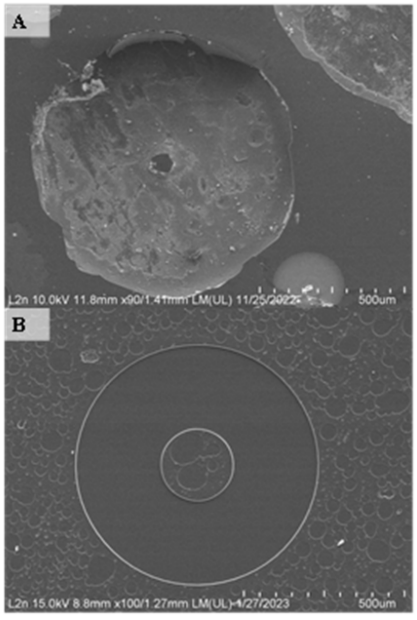

Fig. 9. A) SEM images of electrochemical etched surface B) SEM images of fluorinated plasma etched surface.

Nondirectional etched structures were obtained after performing electrochemical etching (Fig. 9 A) compared to the directionally etched structures obtained using fluorinated plasma etched thickness (Fig. 9 B).

On the SiC electrochemical etched surface, a porous structure is obtained instead to the smooth fluorinated plasma SiC etched surfaces. The trench formed by electrochemical etching with a porous surface obtained in lateral and bottom part is shown in Fig. 10.

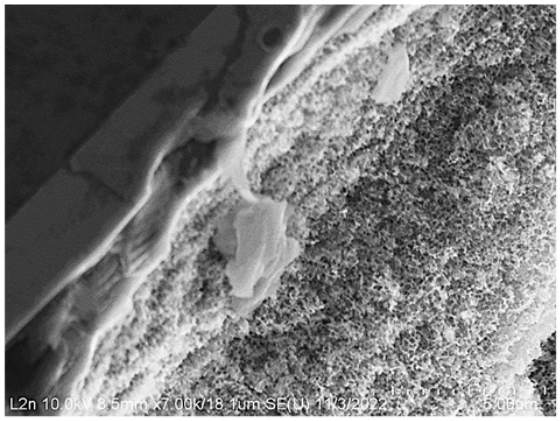

Fig. 10. SEM images of electrochemical etched surface for the n-type SiC.

In order to increase the etching rate, the current applied intensity was increased. Scanning electron microscopic images from the bottom part of the etched surfaces are presented also in Fig. 11 A and B. These results show the increase in the porosity upon increasing the pulsed current from 0.25 A to 1 A.

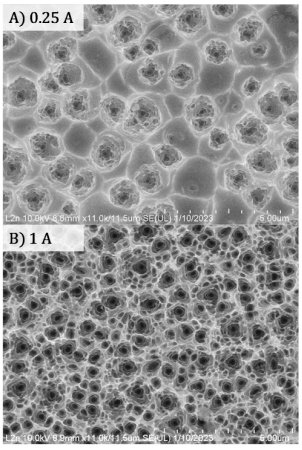

Fig. 11. A) SEM image of the porous etched surface of n-type SiC by regulating the current equal to 0.25 A during electrochemical etching. B) SEM image of the porous etched surface of n-type SiC by regulating the current equal to 1 A during electrochemical etching.

4. Conclusions

A Ni electroplating procedure was applied on activated SiC substrate. Activation of SiC using APTES, followed by Pd treatment, allows for having a more compact and rigid Ni metal on the surface of the SiC substrate. The Ni layer stays rigid and stable even after the plasma etching process, without affecting its thickness except at a few hundreds of nanometers. A considerable SiC etching thickness measured around 30 μm was obtained by applying two 30 min plasma etching process, using SF_6/O_2. Whereas, up to 80 μm etched thickness we could reach using electrochemical etching. Besides, we observed that the increasing of the applied current in the electrochemical etching increases the porosity of the etched surface. This study opens perspectives for having integrated multi-terminal chip made from SiC by performing deep etching to isolate devices.

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