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Editorial: Special Issue on Electronics, Microtechnologies and Materials Science

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This special issue presents a selection of 7 extended contributions of the best papers proposed by the chairpersons of the International Semiconductor Conference – CAS 2023.

The International Semiconductor Conference – CAS 2023, at its 46th edition, is a conference with a wide range of topics, from nanoscience and nanoengineering to photonics, semiconductor devices and integrated circuits, being the only conference organized in Romania in the field of semiconductors. It took place between October 11–13, 2023, in Sinaia, Romania (https://www.imt.ro/cas).

The conference was organized under the aegis of the Electron Devices Society of IEEE (IEEE-EDS), by the National Institute for Research and Development in Microtechnologies – IMT Bucharest, with the support of the Ministry of Research, Innovation and Digitalization.

CAS has been held annually as a national conference since 1978, and as an international conference since 1991. From 1995, the conference became an Institute of Electrical and Electronic Engineering (IEEE) event. IEEE is one of the world's largest international professional societies dedicated to fostering technological innovation and excellence for the benefit of humankind. The conference is included in the IEEE-EDS conference calendar.

The CAS 2023 conference was an important event in the field, which joined together well recognized researchers, academic experts, industry specialists and students to share new ideas, to disseminate innovative, recent advanced research in the field of **micro- and nanotechnologies** and **semiconductor devices**. The conference facilitates the exchange of scientific and technical information.

CAS 2023 joined 203 participants from 79 organizations: 41 universities, 23 research institutions, 15 companies as follow, 125 participants from Romania; 77 participants from abroad, from 24 countries: Austria, Belgium, Bulgaria, Cech Republic, Finland, France, Germany, Islanda, India*, Irland, Italy, Japon, Latvia, Moldova, Norway, The Netherlands, Poland, Portugal, Saudi Arabia, Serbia, Spain, Sweden, USA*, and UK (*authors from India and USA attended the conference online).

The conference program included 3 sessions of invited papers, 11 sessions for oral presentations with 3 sessions for student papers and 4 posters sessions with 1 session for student papers.

101 papers were presented: 10 invited papers, 56 oral presentations, and 35 posters.

Two satellite events took place in parallel: the "Dry Etch Expert Meeting" organized by IMT Bucharest in cooperation with the EuroNanoLab consortium on October 09-10; the "NET4Air" School on Environmental Sensors organised in the frame of the Horizon Europe project NET4Air on October 14.

The conference program included the round table of *"The Microelectronics Ecosystem In Romania – Current Status, Challenges, And Perspectives"*, where important actors from the academic and industrial environment, as well as from funding agencies and institutions, discussed the challenges and the current opportunities in the field of microelectronics, which is a field of national, European and global interest, a key factor for the development of future technologies.

CAS 2023 conference attracted the participation of industry representatives with papers, from Romanian companies (*e.g.*, Infineon Technologies Romania; ON Semiconductor Romania; Continental Automotive; NANOM MEMS SRL) and from abroad (Park Systems Europe, Germany; Cambridge GaN Devices, UK), offering many opportunities for discussions and direct interactions between participants from academic and private entities from Europe and beyond.

In this productive environment, already existing partnerships were consolidated, and the premises for future collaborations were established regarding the realization of new research projects in the field of micro- and nanoelectronics.

The original papers presented at the conference, were accepted after a peer review selection made by the International Program Committee.

The first paper, presented in the Session on Microphotonics & Microwaves by Alina-Cristina Bunea et al., "Passive Radio Frequency Identification Tag with Frequency Doubler and Energy Harvesting", presents the simulation and experimental results obtained for a passive RFID tag based on the integration of microstrip patch antennas and a frequency doubler circuit on the same low-cost FR-4 substrate. The authors focused on the design, fabrication and measurements of a passive harmonic RFID tag operating with an interrogation signal in the 2.5 GHz frequency range. The microstrip antennas and the frequency doubler are hybrid integrated with *Surface Mounted Device* (SMD) on the same *Printed Circuit Board* (PCB) with 105×52 mm overall dimensions. Microstrip patch antennas were designed for operating frequencies in the 2.5 GHz and 5 GHz frequencies ranges and were measured for input matching and radiation gain extraction. The frequency doubler circuit was design using the small signal bias dependent S parameters for the Schottky diode and 3D electromagnetic modeling. Nonlinear simulations were performed in the calculation of the second order harmonic output power and the harvested DC power. A prototype of the proposed harmonic RFID transponder circuit was fabricated using a standard photolithographic process and wet etching of a FR-4 double clad substrate. Circuit blocks design, fabrication and characterizations make possible the demonstration of a passive harmonic tag which takes advantage of the nonlinear characteristic of the Schottky diode, adding energy harvesting features to the backscattering of the second harmonic in the RF identification system. This increase in readout range, as well as the relatively reduced size of (105×52 mm), low manufacturing costs and batteryless operation feature, recommend it for limited accessibility applications across various industry areas. The 2.5 GHz range interrogation frequency facilitates the future integration with common wireless communication systems operating in the sub-6 GHz bands of 5G/6G and Internet of Things technologies.

"On the Modelling Possibilities of Integrated Circuits Behavior Using Active Learning Principles" is the second paper, presented by Vasile Grosu *et al.*, in the Session on Integrated Circuits, Modelling & Microsensors - Student Papers, proposed two Active Learning sampling schemes

that can be used to minimize the number of samples needed for creating reliable metamodels. The authors validated and compared the approaches with classical fixed sampling schemes on a set of synthetic functions, a simulated circuit and a power device. *Active learning* (AL) is an iterative sampling method where the training database is updated based on a selection criterion in order to improve the existing model. Thus, the sampling efficiency is attained through iterations, only the samples that are important in what regards the model accuracy are collected and compared to the fixed sampling schemes that may acquire unnecessary/redundant data. The basic idea behind AL sampling is to focus data gathering efforts on regions of interest where data is more likely to contain valuable information, and reduce sampling in regions where data is unlikely to provide much insight. This can result in significant improvements in the quality and efficiency of data collection, especially in situations where the cost or difficulty of collecting data is high. The paper presents: active learning implementation using neural network Regression, experimental results to assess the capability of AL approaches in modelling the circuit's behavior optimally in what regards the needed number of simulations, when compared with fixed sampling schemes, comparison of sampling algorithms for synthetic functions behavior modelling. There are presented two efficient AL based sampling algorithm that can be used to model circuits or devices behavior by the means of ML regressions in what regards their performance dependence on the design parameters. The main benefit of the presented methods consists in reducing the costs associated with the necessary simulations that are needed to characterize IC behavior. It was shown that the use of the AL sampling methods for creating IC metamodels has strong advantages regarding the data efficiency when compared to the fixed sampling methods and was experimentally proven.

In the third paper, presented in the Session on Modelling & Semiconductor Devices, "Accurate numerical methods for modeling forward characteristics of high temperature capable Schottky diodes", by Gh. Pristavu *et al.*, discusses two algorithms for accurately determining solutions to the transcendental thermionic emission equation, which is the cornerstone of forward electrical behavior in Schottky diodes. The numerical techniques were developed based on the Newton-Raphson and Halley methods. Both methods use distinct forms for the thermionic emission expression, emphasizing robustness against numerical overflows. Parameter initialization, complexity and applicability were presented and discussed for each technique. A comparison is carried out between forward characteristics simulated with the two methods, which are then also used for characterizing real SiC-Schottky diodes. The paper investigates high-fidelity simulation methods for the TE-based conduction mechanism of a Schottky diode over ample temperature ranges. The simulated and experimental results constitute a major step towards implementation of an accurate, automated characterization tool, driven by emerging optimization algorithms. The adequacy of two methods (Newton-Raphson and Halley) for simulating the behavior of practical Schottky diode were analyzed. Forward curves of Schottky diodes with various contacts were measured in encompassing temperature domains. High barrier Ni/4H-SiC and low SBH Ti/4H-SiC and Cr/4H-SiC contacts were selected for analysis. Both methods relied on custom reformulations of the TE expression in order to achieve a form which is robust against numerical overflows. The first method uses the Newton-Raphson algorithm to quickly converge towards an accurate solution with a minimal amount of iterations. This is achieved by reusing previous solutions as initialization for subsequent data points. The second method utilizes Halley's method, which incorporates second-order-derivative information, to reach even faster convergence speed which is further enhanced by its parallel-computing compatibility. Thus, this technique enables the computation of all estimates at the same time.

The paper "Theoretical Studies of Intensity and Phase Based Surface Plasmon Resonance Sensors" (in the Session on Microphotonics & Microwaves), authors: G.A. Bulzan *et al.*, presents the numerical results of reflectivity and phase dependence on the incidence angle for SPR Surface Plasmon Resonance) configurations based on fused silica and BK7 substrate for various wavelengths from visible range. One of the most used configuration, which is also employed in SPR detection, is the so-called "Kreschmann configuration", which consists of a prism with a thin metallic film deposited on one of its surfaces. The intensity and phase response is studied for various wavelengths, and two *refractive index* (RI) values of the analyte (*e.g.*, 1.33 and 1.36). Two different substrate materials, BK7 with a refractive index of approximately 1.51 and fused silica with a refractive index of approximately 1.45 are considered. SPR responses in intensity and phase for various configurations are calculated and the information regarding the optimal internal incidence angle was used to calculate the value of the fixed external incidence angle. The response of the SPR sensor to different values of the medium refractive index has been obtained using a code written in C++ software based on Abeles matrices method; this method allows to evaluate the intensity and phase change of the reflected/transmitted radiation for a multilayered structure. The authors considered four scenarios regarding the materials for prism and the glass slide, respectively, taking in account only the two materials: BK7 and fused silica. They calculated for different wavelength the SPR response in terms of the incident angle, in intensity and in phase. The SPR response in intensity and phase depends strongly on radiation wavelength, substrate type and analyze refractive index. The analysis made at the wavelengths 635 nm, 670 nm and 780 de nm leads to the conclusion that promising results can be obtained for the wavelengths 635 nm, 670 nm and 780 nm in the case of the glass BK7 substrate. In the case of the fused silica substrate we obtained good results for the wavelengths of 670 and 780 nm. The results are important to manufacture low cost simple sensors based on this principle.

The fifth paper, "8-bit DEM-based Feedback Controller applied on an Instrumentation Amplifier", authored by Alex Calinescu *et al.*, was presented in the Session on Integrated Circuits – Student Papers. The all-in-one integration of an accurate instrumentation amplifier, together with an analog-to-digital converter, computational capabilities, and robust communication protocols within a single chip, positions microcontrollers as a competitive low-cost solution for data acquisition, sensing, and control of complex systems. The authors presented a study of a low-cost microcontroller equipped with two operational amplifiers and an analog-to-digital converter. They introduced a versatility in gain options by incorporating a smart digital control circuit, thereby creating a programmable gain instrumentation amplifier. The authors evaluated the feasibility of combining, within a general-purpose microcontroller, the appealing DEM (Dynamic Element Matching), *i.e.*, very accurate resistive ratios ranging between 1 and 15, with the associated versatile and scalable interrupt-aware digital controller. Given a mixed-signal system, a hybrid evaluation environment has been implemented to perform relevant test-benches for assessing the system's performance, *i.e.*, DEM controller, muxes, OpAmps, with respect to relevant metrics for integrated digital and mixed-signal circuits, *i.e.*, energy, delay, footprint, precision. The gain precision of a typical amplifier is improved by more than 1800 times, with the error converging to as low as 10s of ppm, for gaussian mismatch distribution between –1% and 1% with the cost of DEM digital circuitry which adds about 30000 μm2 of chip area and consume 194 μA, when implementing our design in a commercial 180 nm technology.

Cosmin Romanitan *et al.* presented in the sixth paper, "Microstructure of VO_2 Thin Films Synthesized by Pulsed Laser Deposition", in the Section on Nanoscience & Nanoengineering, their work related to deposition of *Vanadium oxide* (VO_x), by *pulsed laser deposition* (PLD) at

low partial oxygen pressure (∼10 mTorr). Since *Vanadium oxide* (VO_x) compounds have unique properties, which are strongly linked with the actual oxidation state, and which can be exploited for a wide range of applications, such as charge storage, photodetectors, sensors, smart windows or photocatalysis, they investigated the experimental manufacturing of VO_2 and analysed their properties through electrical, AFM, X-ray caracterizations. The paper treats the deposition of $VO_2/SiO_2/Si$ by PLD in one-step process, which was optimized, without any post-thermal processes. Their findings indicated that the obtaining of VO_2 layers with high crystal quality (low dislocation density) need the use of high deposition temperatures. Their results showed that the optical band gap is affected by the dislocation density, being reported a decrease from 0.9 eV to 0.6 eV, at a decreasing of dislocation density from 3 to 0.9^x 1011 cm^{-2}. Also, the electrical measurements pointed out that the dislocations in VO_2 induce different features in the dependence of the resistance with temperature. C. Romanitan *et al.* consider that it is essential to develop suitable growth procedures, capable of crystalline VO_2 synthesis, without post-annealing treatments. A detailed understanding of the relationship between the growth parameters and the resulted microstructure is necessary in order to explain different optical and electrical properties. The investigations in vanadium oxide films obtained by PLD at low oxygen pressure pointed out the possibility to obtain crystalline VO_2 thin films in a one-step process, starting from the ablation of a pure V_2O_5 target by PLD. The XRD results indicate that the unit cell parameters are not affected by the substrate temperature or number of pulses. The mean crystallite size, lattice strain or dislocation density are affected by the PLD growth parameters.

The 7th paper, "Improved SPI Controller Based on Scan Architecture" (in the Session on Integrated Circuits – Student Papers), authored by Ionelia-Bianca Brezeanu *et al.*, suggests a high performance, digital serial controller having a self-test-based architecture. A standard architecture able to achieve the targeted functionality was modified in order to contain the test mode circuitry for testability improvements. After the importance of creating digital architectures adapted for testability is underlined, frequency serial controller for analog switches is presented. This block was adjusted for test reasons and implemented into a 3 V CMOS technology. A first implementation of the serial controller was designed in a 180 nm CMOS technology, being able to operate with frequencies up to 55 MHz, for supply voltages between 2.5 – 5.5 V and within a temperature range of 40 °C ÷ 125 °C. Verifications were run on schematic and layout of this circuit for validating it. The building parts of the proposed block are finite state machine meant to decode the instructions and provide internal signals for updating the registers bank, circuitry for providing and storing the default output code for serial output, bits counter, four storage registers (register at address 0×01 is controlling the switches) and a reset register. All logic transitions of the data input are being synchronized with the SCK clock signal and all outputs are expected to reach their final steady state values in one clock period after the changes in the inputs. This required the fact that the delay of the combinational circuitry to be much lower than the clock period, along with implementing a robust clock tree structure for driving the internal clock signals to the intended flip-flops. The results were obtained using special CAD tools dedicated to defects analysis on mixed signal integrated circuits, without requiring scan circuitry for evaluating the design. An improved SPI controller used in analog switches applications was designed in two architectures: the first one targeted serial functionality able to operate at 55 MHz and a second one derived from the previous, adjusted for testability reasons. For the second implementation, scan insertion was performed in order to adapt the initial architecture to a self-test capable version. The improved SPI controller based on scan architecture was designed in a CMOS 65 nm technology. This design was validated through digital functionality simulations and timing analysis.

The layout of the digital block was done and a top-level floorplan containing the input-output pad structures is implemented.

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We hope that the readers will find interesting the scientific contributions of this special issue in the fields of electronics, micro-nano technologies and materials science.

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Dr. Raluca Müller – IMT Bucharest, and Dr. Miron Adrian Dinescu – IMT Bucharest, Guest Editors