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Near-optimal March Tests for Three-Cell and Four-Cell Coupling Fault Models in Random-Access Memories

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Abstract. This paper addresses the problem of testing $n \times 1$ RAMs in which complex models of unlinked static three or four-cell coupling faults are considered. As in other papers, it is assumed that only physically neighboring memory cells could be involved in a three or four-cell coupling fault. For this reason, these fault models can also be considered to be of the neighborhood pattern sensitive type. As extensions of the well-known model of all unlinked static two-cell coupling faults, the fault models addressed in this paper are complex including faults sensitized by a transition write operation as well as faults sensitized by a non-transition write or a read operation. For these complex models, near-optimal multirun march tests are proposed. This optimality assessment is based on the fact that, for any group of cells corresponding to the considered fault model, the state graph is completely covered, and each arc is traversed only once, which means that the graph is of the Eulerian type. Additional write operations are only required for data background changes.

Key-words: Eulerian graph; four-cell coupling; multirun march tests; near-optimal tests; RAM testing; three-cell coupling.

1. Introduction

In this paper, the authors address two complex fault models in $n \times 1$ random-access memories, namely, unlinked static three-cell coupling faults and unlinked static four-cell coupling faults. These complex models involving three or four coupled cells are extensions of the well-known model of all static unlinked two-cell coupling faults, first presented in [1], and for which a memory test of length $22n$ was proposed. Minimal march tests for this model of two-cell coupling faults requiring only $18n$ operations are reported in [2].

Based on the set of fault primitives (FPs) describing the model of all static two-cell coupling faults presented in [1], a FP-based description of a three-cell coupling model is presented in [3] and also considered in [4] for which dedicated memory tests are reported. Such a model is also considered in this paper, and in addition, a four-cell coupling fault model is addressed. For both these complex fault models, near-optimal march tests are proposed.

According to the classification of memory faults, as presented for example in [1], [5]-[7], the 'static faults' class refers to those faults sensitized by performing at most one memory operation, while the 'dynamic faults' class refers to those faults sensitized by two or more operations performed sequentially. In compliance with the same taxonomy presented in [8] or [9], for example, two coupling faults are said to be unlinked when they do not influence each other. In this paper, the class of unlinked static coupling faults is addressed.

A three-cell coupling fault model was first introduced by Nair, Thatte and Abraham [10]. For this model where the coupling cells can be anywhere in memory, the authors proposed a test algorithm of length $n + 32n \log_2 n$. A few years later, Papachristou and Sahgal improved the memory test procedure dedicated to this model by providing a test algorithm of length $37n + 24n \log_2 n$ [11]. To cover this model, both algorithms use testing techniques based on dividing the memory into halves with respect to a specific address bit.

Two other more efficient test algorithms for this model, denoted S3CTEST and S3CTEST2, are given by Cockburn [12]. To cover models with multi-cell coupling faults, Cockburn proposes a multi-stage testing technique that uses different memory data backgrounds (now called 'multirun memory testing'). The S3CTEST and S3CTEST2 tests apply this technique. Compared to previous tests, S3CTEST and S3CTEST2 require fewer operations. For example, S3CTEST is a test of length $5n \log_2 n + 22.5n$.

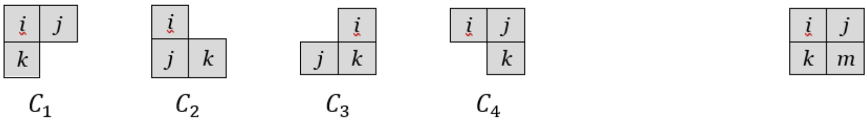
The authors assume in all the papers discussed above that three-coupled cells can be anywhere in memory. For this reason, the tests are quite long, falling into the $O(n \log_2 n)$ complexity class.

To reduce the length of the tests, Caşcaval and Bennett [13] limit themselves to a model where only physically neighboring memory cells could be involved in a three-cell coupling fault. There are four possible configurations for three physically adjacent cells arranged in a corner, as shown in Fig. 1. For this more realistic three-cell coupling model, the authors present a multirun march test algorithm (called MT) of $O(n)$ complexity that requires $38n$ operations.

An improved march test algorithm dedicated to a three-cell coupling model, called $MT-$ $-R3CF$, requiring only $30n$ operations is given by Caşcaval, Bennett and Huţanu [14]. Furthermore, the coupling model considered in [14] also covers two other adjacent cell configurations. More precisely, in addition to the four configurations arranged in a corner presented in Fig. 1 a), the model includes three neighboring cells arranged in a row or a column.

All the test algorithms mentioned so far cover restricted coupling models where a memory fault is only sensitized by a transition write operation to a cell (a write operation for changing the state of the addressed cell).

With the great increase in RAM memory integration density and the increase in operating frequency, the range of memory defects has expanded considerably [15], [16]. As a result, around the 2000s, extended models of coupling faults were proposed to cover new memory defects, by including classes of faults sensitized by reading or writing operations without changing the state of the addressed cell. These new classes of faults are: write disturb coupling, read destructive coupling, deceptive read destructive coupling or incorrect read, as defined in [5], and also addressed in other papers including [1]-[4], [8], and [16]-[18].



a) Three-cell configurations b) Four-cell configuration

Fig. 1. Configurations with three or four physically adjacent memory cells.

As previously mentioned, an FP-based description of the extended three-cell coupling model is presented in [3] and also considered in [4]. The FP set for this model is also presented in detail in [19, Table 1], where some useful considerations are added on how this model can be covered. For this extended model, the authors devise a test algorithm, March SR3C, requiring $66n$ operations. A more efficient march memory test, MT-SR3C, requiring only $54n$ operations, able to cover this model of unlinked static three-cell coupling faults is reported in [4]. But with all that reduction from $66n$ to $54n$ operations, this memory test is not optimal either. An optimal test for this model with six configurations of three physically adjacent cells is still awaited.

This paper addresses an extended three-cell coupling model, described by a large set of FPs presented in [19], which covers the four configurations of three physically adjacent cells arranged in a corner, as shown in Fig. 1(a). For this model, a near-optimal march test of length $37n$ is proposed.

A four-cell coupling fault model is also addressed in this paper. As an extension of the two- and three-cell coupling models, the four-cell coupling model includes a wide range of fault types. Specifically, the model includes faults sensitized by a transition write operation performed in a coupled cell group, as considered in [14], but also faults sensitized by a non-transition write operation or a read operation. A selection from the set of FPs describing this extended model of four-cell coupling is also presented in detail in [19, Table 2].

As in [14], the four-cell coupling model considered in this paper is limited to neighboring memory cells arranged in a square, as shown in Fig. 1 (b). It should be noted that the importance of this configuration of four neighboring cells is also explained by the fact that, at the layout level, in some implementations, four cells arranged in a square share the same ground path [16]. For this four-cell coupling model, a near-optimal multirun march test of length $73n$ is given in this paper.

The models discussed here can also be considered of neighborhood pattern-sensitive fault (NPSF) type [20]-[24]. Nevertheless, in these models, any cell in the group may be a victim cell not just the central cell, as it is usually considered in the NPSF model. Testing for NPSF models is covered extensively in Mrozek's book [22].

To reduce the length of tests dedicated to multi-cell coupling or NPSF models, other authors propose a multirun technique in which various address sequences are randomly generated [25], [26]. But, in this way, the fault model is only partially covered.

The remainder of this paper is organized as follows. Section 2 presents assumptions, notations, and some preliminary considerations related to multirun memory tests, or to the necessary and sufficient conditions for detecting memory coupling faults. Section 3 describes a new memory test for a three-cell coupling model, while Section 4 presents a memory test for a four-cell coupling model. The concluding remarks are included in Section 5.

2. Assumptions, Notations and Preliminaries

2.1. Assumptions

As in any paper dedicated to NPSFs, it is assumed that the scramble map is fully known, so that a march memory test using different data backgrounds can be applied based on the physical address information. Naturally, in the memory under testing, one or more groups of coupled cells may exist. As in [3], [4], [10]–[14], it is assumed that the groups of coupled cells are disjoint.

2.2. Notations

The notations commonly used to describe the memory operations are presented in Table 1.

Table 1. Memory operations

Operation	**Description**
$r0\,(r1)$	Operation of reading a memory location and checking the read value by comparing it with the specified logical value 0 (1).
r	Operation of reading a memory location and checking the read value without explicitly specifying the expected value.
$w0\,(w1)$	Operation of writing the logical value 0 (1) to a memory cell.
$0w0\,(1w1)$	Operation of writing the logical value 0 (1) to a memory cell without changing the state of the addressed cell (non-transition write operation).
$0w1\,(1w0)$	Write operation to change the state of the addressed cell by a transition from 0 to 1 (from 1 to 0).
w_t	Write operation to change the state of the addressed cell (transition write operation) without explicitly indicating the transition type ($0w1$ or $1w0$, as appropriate).
w_{nt}	Write operation maintaining the state of the addressed cell (non-transition write operation) without explicitly indicating the logical value used ($0w0$ or $1w1$, as appropriate).
$\uparrow, \downarrow$	A change of logical state in the victim cell, from 0 to 1 or vice versa, as appropriate, by sensitizing a memory fault (i.e., a memory error).

2.3. Preliminaries

A march test is composed of a set of march elements and each march element contains a sequence of memory operations and a symbol that specifies the order in which the memory cells are accessed. Specifically, given a sequential enumeration of all memory addresses, the symbol $\Uparrow$ indicates traversing these addresses in ascending order, while the symbol $\Downarrow$ indicates traversing them in reverse order. Moving to the next cell, according to the address sequence, is done only after performing all operations on the current cell, according to the march element.

In the case of a multirun testing, a specific march test is repeatedly applied to different data backgrounds. A data background (i.e., a memory initialization) is obtained by multiplying a data pattern in memory, horizontally and vertically. Such a technique is applied for any NPSF model.

To detect a fault, a memory test must first sensitize the fault through a certain memory operation and then read the affected cell (also called victim cell) to observe the error. As pointed out in [8], to verify the ability of a memory test to detect all unlinked static coupling faults corresponding to a model, it is sufficient to verify the test's ability to detect the FPs describing that model. But in [19] it is shown that FPs cover all memory operations that can be performed in a cell group corresponding to that model. Consequently, for a coupling fault model, in terms of satisfying the sensitization condition, a memory test must cover the state graph (transition graph or full state graph, as appropriate) for any group of cells corresponding to that model. Under this aspect, a memory test is optimal if, for any group of cells, all operations in the state graph are performed only once (i.e., for any group of cells, the state graph is Eulerian).

As also presented in [3], [4] or in [16], to detect errors resulting from memory fault-sensitizing, two necessary and sufficient observability conditions must be met:

- OC_1 A memory cell must be read after performing a fault sensitizing operation or after a sequence of sensitizing operations performed sequentially to check that the last operation was carried out correctly;
- OC_2 Before writing to a cell, it must first be read, to check that a change of state has not occurred as a result of an operation previously performed in another possibly aggressor cell.

3. Near-Optimal March Test for Three-Cell Coupling Fault Model

This section addresses the coupling fault model involving groups of three physically neighboring cells arranged in a corner, as shown in Fig. 1 (a). The fault model consider in this section is an extended coupling model, including both faults sensitized by transition write operations and faults sensitized by non-transition write operations or by read operations, as described in detail in [3], [19]. To cover this complex coupling model, this paper proposes a memory test, $MT-$ $-3CCF$, in which two march elements are applied four times on different data backgrounds. The description of this new multirun march memory test algorithm is given in Fig. 2, and the four patterns used for memory initialization are shown in Fig. 3. In this description, BGC_1 indicates the primary memory initialization sequence, while BGC, $i = 2, 3, 4$, represent test sequences with a change of data background, according to the patterns shown in Fig. 3.

Note that, any change of data background involves status update only for half of the memory cells. On the other hand, in order to satisfy the OC_2 observability condition, any write operation to change the state of a memory cell is preceded by a read operation. Thus, the initialization sequence BGC_1, which is of the form $\Uparrow (w0)$, involves n write operations, while a test sequence with background change, BGC_i, $i = 2, 3, 4$, requires $n/2$ read operations and $n/2$ write operations.

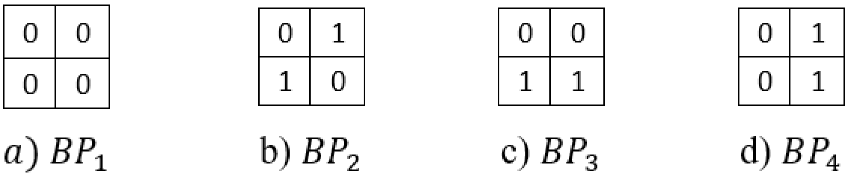
With these specifications, the length of the $MT - 3CCF$ memory test is given by the following equation:

$$L = 4 \times (n + 8n) + n = 37n. \tag{1}$$

Specific to such a multirun test is the dependency between the value of a memory cell and its address. It should be noted that background patterns of size 2×2 allow a simple implementation of the test algorithm. For example, on a background change, the logical value for the current cell is generated based on the least significant bit (LSB) of the row address, $A_r[0]$, and/or the column address, $A_c[0]$, as shown in Table 2.

$MT - 3CCF = \langle \{ \ BGC_i;$
$\Uparrow (r, \mathbf{w_t}, w_{nt}, r);$
$\Uparrow (r, \mathbf{w_t}, w_{nt}, r); \}, \ \ i = 1,2,3,4 \ ;$
$\Uparrow (r); \rangle$

Fig. 2. $MT - 3CCF$ memory test.



a) BP_1 b) BP_2 c) BP_3 d) BP_4

Fig. 3. Background patterns used by $MT - 3CCF$.

Table 2. The value of a cell according to the pattern and its address

BP_1 – solid data	BP_2 – checkerboard	BP_3 – row stripe	BP_4 – column stripe
0	$A_c[0] \oplus A_r[0]$	$A_r[0]$	$A_c[0]$

The ability of the $MT - 3CCF$ memory test to cover this extended three-cell coupling fault model is discussed in the following.

Theorem 1. The $MT - 3CCF$ memory test is able to detect all unlinked static faults of this three-cell coupling model.

Proof: Let $\boldsymbol{G}$ be an arbitrary group of three neighboring memory cells that matches one of the four coupling configurations, C_1, C_2, C_3, or C_4. Considering the order in which these cells are accessed on a memory scan in ascending address order, cells in group $\boldsymbol{G}$ are denoted by i, j, and k as illustrated in Fig. 1 (a). The ability of the $MT - 3CCF$ test algorithm to sensitize and observe any fault that may affect a cell in a cell group $\boldsymbol{G} = \{i, j, k\}$ is demonstrated in the following.

I. MT – 3CCF is able to sensitize any fault in a ***G*** *– coupled cell group*

To prove this statement, it is shown here that during the memory testing, $MT - 3CCF$ performs all possible operations in the group of cells $\boldsymbol{G} = \{i, j, k\}$. In other words, it is shown that $MT - 3CCF$ completely covers the graph of states describing the normal operation of these cells. The proof is conducted in two stages: the first one focuses on transition write operations, while the second one addresses read and non-transition write operations.

Stage 1. Transition write operations: A transition write operation must change the state of the addressed cell. Such write operations are highlighted in bold in the test description in Fig. 2. After a background change, the state of a group of cells depends on the configuration, the background pattern, and the position of the group in the memory array. All possible cases are illustrated in [19, Fig. 6].

Table 3 presents the initial state vectors for a group of three cells $\boldsymbol{G} = \{i, j, k\}$ in all cases, as highlighted in [19].

Table 3. Initial state vectors for a group of cells $\boldsymbol{G} = \{i, j, k\}$ depending on configuration, background pattern and its position.

	BP_1	BP_2	BP_3	BP_4
C_1	(0 0 0)	(0 1 1)	(0 0 1)	(0 1 0)
		(1 0 0)	(1 1 0)	(1 0 1)
C_2	(0 0 0)	(0 1 0)	(0 1 1)	(0 0 1)
		(1 0 1)	(1 0 0)	(1 1 0)
C_3	(0 0 0)	(1 1 0)	(0 1 1)	(1 0 1)
		(0 0 1)	(1 0 0)	(0 1 0)
C_4	(0 0 0)	(0 1 0)	(0 0 1)	(0 1 1)
		(1 0 1)	(1 1 0)	(1 0 0)

In Table 3 it can be seen that by initializing the memory and then by the three background changes, any group of cells $\boldsymbol{G} = \{i, j, k\}$ of the considered type is brought to the following four initial states, listed in a non-relevant order:

1. $\begin{pmatrix}0 & 0 & 0\end{pmatrix}$,
2. $\begin{pmatrix}1 & 0 & 0\end{pmatrix}$ or its complementary state $\begin{pmatrix}0 & 1 & 1\end{pmatrix}$,
3. $\begin{pmatrix}0 & 1 & 0\end{pmatrix}$ or its complementary state $\begin{pmatrix}1 & 0 & 1\end{pmatrix}$,
4. $\begin{pmatrix}0 & 0 & 1\end{pmatrix}$ or its complementary state $\begin{pmatrix}1 & 1 & 0\end{pmatrix}$.

With respect to a group of cells, two states are complementary if all bits in the state vectors are reversed. In a cube-shaped state graph, two complementary states are represented by two nodes that are not in the same plane. It should be noted that, starting from a given initial state, by applying the first march element, a group of cells is brought (through the transition write operations denoted by w_t) to the complementary state. Then, by applying the second march element, the group of cells is returned to its initial state. Moreover, regardless of whether one starts with a given initial state or its complementary state, by applying the two march elements, in a group of cells the same transitions are made, but in a different order.

With these specifications, the transitions performed in a cell group $\boldsymbol{G} = \{i, j, k\}$, when applying this march memory test, are highlighted in [19, Fig. 7] in different colors. In conclusion, $MT - 3CCF$ performs all transitions in the state graph, for any group of three physically adjacent cells, in any of the four configurations considered in this model. Moreover, each of these transitions is performed only once.

Stage 2. Read and non – transition write operations: According to the test description in Fig. 2, after a state is reached by a transition write operation (w_t), the memory test performs two more operations without leaving the current state: a non-transition write operation (w_{nt}) and a read operation (r). This means that during memory testing, all normal operations are performed in any group of cells $\boldsymbol{G} = \{i, j, k\}$. Therefore, the $MT - 3CCF$ memory test is able to sensitize any fault in a group of three coupled cells.

II. $MT - 3CCF$ *detects any sensitized fault in a group* **G** *of coupled cells*

In this test, a march element starts and ends with a read operation. For a background change, any write operation to change the state of a memory cell is preceded by a read operation. The test also ends with a final check. Thus, regarding the fulfillment of the two observability conditions, OC_1 and OC_2, the only question is related to the fact that the test performs two successive write operations in the same cell (w_t, w_{nt}). The explanation for this simplification is as follows: if the first write operation fails and thus the addressed cell retains its old logical value, the second write operation is actually a new attempt to change the state of the cell. In fact, there is a sequence of sensitizing operations here, and no further verification is required between these two successive writes. For a direct and explicit check, in [19, Fig. 8] all the operations performed in a group of cells $\boldsymbol{G} = \{i, j, k\}$are presented when applying the $MT - 3\,CCF$ memory test.

The write operations used for background changes (those written in green), along with the associated read operations, are enclosed in square brackets to highlight that these operations are sometimes executed, sometimes not, depending on the cell address and the background pattern. Read operations written in red are used to detect possible errors, while read operations highlighted in blue are used for both fault sensitizing and error detection. With this demonstration of the fulfillment of the conditions necessary to detect those errors resulting from memory fault sensitization, the proof of Theorem 1 is complete.

Remark 1. For any group of cells that corresponds to the four configurations, the state graph is completely covered, and furthermore, each transition is performed only once, which means that the state graph is Eulerian. The only redundant operations are used for background changes, so with only $3n$ additional operations, this memory test can be said to be near optimal.

Remark 2. Two other memory tests dedicated to a three-cell coupling fault model, named $MT - SR3C - 1$ and $MT - SR3C - 2$, of the same length $37n$ but different in structure, are presented in [4]. Each of the two test algorithms is capable of covering three configurations of three physically adjacent cells, two configurations arranged in a corner and one in a row or in a column.

Compared to these, the memory test proposed in this paper, $MT - 3\,CCF$, is more efficient because it covers the four configurations of three physically adjacent cells arranged in a corner and is simpler to implement in a BIST-RAM type structure.

For a restricted three-cell coupling model, where it is assumed that a fault is sensitized only by a transition write operation, a near optimal multirun memory test called $MT - R3\,CCF$ is proposed, as presented in Fig. 4.

$$\boxed{MT - R3CCF = \langle\, \{BGC_i;\ \Uparrow (r, w_t); \Uparrow (r, w_t);\}, i = 1, 2, 3, 4\ ;\ \Uparrow (r);\, \rangle}$$

Fig. 4. $MT - R3CCF$ memory test.

The $MT - R3\,CCF$ memory test is $21n$ long, as shown in the following equation. For comparison, for the two-cell coupling fault model, an optimal memory test is $18n$ long [2].

$$L = 4 \times (n + 4n) + n = 21n. \qquad (2)$$

4. Near-Optimal March Test for Four-Cell Coupling Fault Model

As mentioned in the Introduction, this paper refers to the coupling fault model involving groups of four physically neighboring cells arranged in a square, as shown in Fig. 1 (b). As an extension of the extended three-cell coupling models, this four-cell coupling model also covers both faults sensitized by transition writes and faults sensitized by reads or non-transition writes. As with the three-cell coupling model, any cell in the four-cell group can be a victim cell. As mentioned in the Introduction, a FP-based description of this model can be found in [19].

To cover this model of four-cell coupling faults, the same memory test technique is adopted, where one or more march elements are applied many times on different data backgrounds. But, compared to the three-cell coupling model, in this case another march element type is required. Specifically, the state graph can no longer be covered in the same way as in the previous model.

For this complex fault model, a near-optimal memory test called $MT - 4CCF$ is proposed with the description presented in Fig. 5. In this description BGC_1 is the primary memory initialization sequence, as the form $\Uparrow (w0)$, and BGC_i, $i = 2, 3, ..., 8$ represent background changing sequences. The patterns used for data background are shown in Fig. 6.

$$MT - 4CCF = \langle \{ BGC_i; \Uparrow (r, \mathbf{w_t}, w_{nt}, r, r, \mathbf{w_t}, w_{nt}, r); \}, i = 1, 2, \cdots, 8; \Uparrow (r); \rangle$$

Fig. 5. $MT - 4CCF$ memory test.

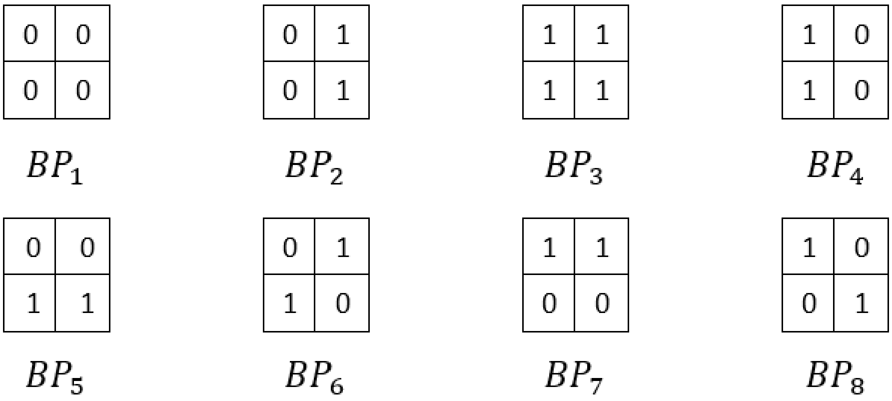


Fig. 6. Background patterns used by $MT - 4CCF$.

As can be seen in Fig. 6, for a background change, only half of the memory cells require a state change. In order to satisfy the OC_2 observability condition, a write operation to change the state of a memory cell is preceded by a read operation. Since the first memory initialization sequence involves n write operations, and then any background change sequence requires $n/2$ read operations and $n/2$ write operations, the test length is given by the following equation:

$$L = 8 \times (n + 8n) + n = 73n. \tag{3}$$

The ability of the $MT - 4CCF$ memory test to cover this four-cell coupling fault model is discussed in the following.

Theorem 2. The $MT - 4CCF$ memory test is able to detect all unlinked static faults of this extended four-cell coupling model.

Proof: Let $\boldsymbol{G} = \{i, j, k, m\}$ be an arbitrary group of four physically neighboring memory cells arranged in a square, as shown in Fig. 1(b). Cells in group $\boldsymbol{G}$ are identified by i, j, k, and m, depending on the order in which they are accessed in a memory scan.

The ability of the $MT - 4CCF$ memory test to sensitize and observe any fault that may affect a cell in a cell group $\boldsymbol{G} = \{i, j, k, m\}$ is demonstrated in the following.

*I. MT – 4CCF is able to sensitize any possible fault in a **G** – group of cells*

It is needed to show that $MT - 4CCF$ completely covers the state graph corresponding to a **G**-group of cells.

But first of all, it should be noted that compared to the $MT-3CCF$ memory test, in this case, the state graph is traversed in a different way. To illustrate this aspect, the operations performed in a **G**-group of cells by the first march element are shown in [19, Fig. 11]. In essence, the portion of the state graph shown in [19] highlights the fact that from the initial state, through round trips, four neighboring nodes that differ by a single bit are visited, but distant (non-adjacent) nodes that differ by two or more bits cannot be reached.

Checking the state graph coverage is done in two stages: transitions from one state to another are focussed in the first stage, and operations that do not involve transition between states (i.e., read and non-transition write operations) are focussed in the second stage.

Stage 1. Transition write operations: The initial state for a **G**-group of cells after a background change depends on the background pattern and the position of the group in the memory cell array. All cases to be considered are illustrated in [19, Fig. 12].

The initial states for any group $\boldsymbol{G} = \{i, j, k, m\}$ after memory initialization and background changes are presented in Table 4.

Note in this table that any two initial states differ by at least two bits, and as a result, in the state graph, the nodes associated with these initial states are not neighbors. Since the $MT - 4CCF$ memory test executes the march element eight times, from different initial states, and any two initial states differ by at least two bits, it follows that 64 different transitions are executed in group **G** (*i.e.*, all 64 possible transitions). In conclusion, the $MT - 4CCF$ memory test covers the entire state transition graph for any group of four physically adjacent cells. Moreover, each transition in this graph of states is performed only once, as illustrated in [19, Fig. 13].

Table 4. Initial state vectors for any group of cells $\boldsymbol{G} = \{i, j, k, m\}$ after memory initialization and background changes

BGC_1	BGC_3	BGC_2 and BGC_4	BGC_5 and BGC_7	BGC_6 and BGC_8
(0 0 0 0)	(1 1 1 1)	(0 1 0 1), (1 0 1 0)	(0 0 1 1), (1 1 0 0)	(0 1 1 0), (1 0 0 1)

Stage 2. Read and non-transition write operations: From the test description and from the graph shown in [19, Fig. 11], it should be noted that after reaching a new state through a transition into a cell (w_t), the memory test performs a non-transition write operation (w_{nt}) and then a read

operation (r) to the same cell. This means that during memory testing, all normal operations are performed in a group of cells $\boldsymbol{G} = \{i, j, k, m\}$. Therefore, the $MT-4CCF$ memory test is able to sensitize any fault in a group $\boldsymbol{G}$ of four coupled cells.

II. $MT-4CCF$ *detects any sensitized fault in a group* $\boldsymbol{G}$ *of coupled cells*

For a direct and explicit verification of the fact that the $MT-4CCF$ test fulfills the observability conditions (OC_1 and OC_2) for detecting all possible errors resulting from memory fault sensitization, in [19, Fig. 14] all the operations performed in a group of cells $\boldsymbol{G} = \{i, j, k, m\}$ are presented when applying this multirun march memory test.

When describing the memory test in Fig. 5, read operations highlighted in red are used to detect possible errors, while the other read operations written in blue are used both for sensitizing possible memory faults and for detecting memory errors.

In terms of meeting the observability conditions, the only question concerns the fact that the test performs two successive writes to the same cell (w_t, w_{nt}). But, the explanation for this simplification that does not affect the error detection capability is given in the previous section when the performance of the $MT-3CCF$ memory test was analyzed.

With the verification of the fulfillment of the second condition, which concerns the ability to detect possible errors resulting from the sensitizing of memory faults, the proof of Theorem 2 is complete.

Remark 3. With this memory test, for any group of four cells arranged in a square, the state graph is completely covered, and furthermore, each fault-sensiting operation is performed only once, which means that the state graph is Eulerian. Since the additional operations are only used for background changes, $MT-4CCF$ can be said to be a near-optimal memory test.

5. Conclusions

For the two memory fault models of three-cell and four-cell coupling, near-optimal multirun march tests were proposed. With respect to these tests, two aspects should be noted: 1) relating the fulfillment of the condition of fault sensitization, for any group of cells corresponding to the fault model, each arc in the state graph is traversed only once, and that means that the state graph is Eulerian; and 2) between two writes of the form w_t, w_{nt}, the addressed cell is not checked and this simplification does not affect the test's ability to detect memory errors.

For the two fault models, different march elements are required to detect all the faults. In both memory tests, $MT-3CCF$ and $MT-4CCF$, the memory is traversed in one direction, which simplifies the implementation of address counters in a BIST-RAM type structure.

The ability of each of these two memory tests to cover the considered fault model was also verified by simulation. For faults sensitized by transition write operations, the TRAP interrupt facility was used to simulate memory errors. Dedicated simulation programs were required for the other failures.

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References

[1] S. HAMDIOUI, A.-J. van de GOOR and M. RODGERS, *March SS: A test for all static simple RAM faults*, Proceedings of IEEE Workshop on Memory Technology, Design and Testing, Isle of Bendor, France, 2002, pp. 95–100.

[2] G. HARUTUNYAN, V. A. VARDANIAN and Y. ZORIAN, *Minimal march tests for unlinked static faults in random access memories*, Proceedings of 2005 IEEE VLSI Symposium, Palm Springs, CA, USA, 2005, pp. 53–59.

[3] P. CAŞCAVAL and D. CAŞCAVAL, *March SR3C: A Test for a reduced model of all static simple three-cell coupling faults in random-access memories*, Microelectronics Journal **41**(4), 2010, pp. 212–218.

[4] P. CAŞCAVAL and D. CAŞCAVAL, *March test algorithm for unlinked static reduced three-cell coupling faults in random-access memories*, Microelectronics Journal **93**, 2019, paper 104619.

[5] A.-J. van de GOOR and Z. AL-ARS, *Functional faults models: A formal notation and a taxonomy*, Proceedings of 2000 IEEE VLSI Test Symposium, Montreal, Canada, 2000, pp. 281–289.

[6] S. HAMDIOUI, Z. AL-ARS, A.-J. van de GOOR and M. RODGERS, *Dynamic Faults in Random-Access-Memories: Concept, Fault Models and Tests*, Journal of Electronic Testing. Theory and Applications **19**(4), 2003, pp. 95–205.

[7] D. HAYRAPETYAN and A. MANUKYAN, *Modeling dynamic single-cell and coupling faults via automata models*, Proceedings of 2017 International Conference on Computer Science and Information Technologies, Yerevan, Armenia, 2017, pp. 65–68.

[8] S. HAMDIOUI, Z. AL-ARS, A.-J. van de GOOR and M. RODGERS, *Linked faults in random access memories: concept, fault models, test algorithms, and industrial results*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **23**(5), 2004, pp. 737–757.

[9] A. BOSIO, S. DI CARLO, G. DI NATALE and P. PRINETTO, *March AB - a state-of-the-art march test for realistic static linked faults and dynamic faults in SRAMs*, IET Computers & Digital Techniques **1**(3), 2007, pp. 237–245.

[10] C. NAIR, S. M. THATTE and J. A. ABRAHAM, *Efficient Algorithms for Testing Semiconductor Random-Access Memories*, IEEE Transactions on Computers **C-27**(6), 1978, pp. 572–576.

[11] C. A. PAPACHRISTOU and N. B. SAGHAL, *An Improved Method for Detecting Functional Faults in Random-Access Memories*, IEEE Transactions on Computers **C-34**(2), 1985, pp. 110–116.

[12] B. F. COCKBURN, *Deterministic Tests for Detecting Single V-Coupling Faults in RAMs*, Journal of Electronic Testing: Theory and Applications **5**(8), 1994, pp. 91–113.

[13] P. CAŞCAVAL and S. BENNETT, *Efficient march test for 3-coupling faults in random-access memories*, Microprocessors and Microsystems **24**(10), 2001, pp. 501–509.

[14] P. CAŞCAVAL, S. BENNETT and C. HUŢANU, *Efficient march tests for a reduced 3-coupling and 4-coupling faults in RAMs*, Journal of Electronic Testing. Theory and Applications **20**(2), 2004, pp. 227–243.

[15] R. D. ADAMS and E. S. COOLEY, *Analysis of a deceptive read destructive memory fault model and recommended testing*, Proceedings of 1996 IEEE North Atlantic Test Workshop, Hanover, NH, USA, 1996, pp. 1–6.

[16] R. D. ADAMS, *High Performance Memory Testing: Design Principles, Fault Modeling and Self-Test*, Springer, New York, NY, USA, 2003.

[17] N. A. ZAKARIA, W. Z. W. HASSAN, I. A. HALIN, R. M. SIDEK and X. WEN, *Fault Detection with Optimum March Test Algorithm*, Journal of Theoretical and Applied Information Technology **47**(1), 2013, pp. 18–27.

[18] A. Z. JIDIN, R. HUSSIN, L. W. FOOK and M. S. MISPAN, *A review paper on memory fault models and test algorithms*, Bulletin of Electrical Engineering and Informatics **10**(6), 2021, pp. 3083–3093.

[19] P. CAŞCAVAL and D. CAŞCAVAL, *RAM Testing Considerations on Three-Cell and Four-Cell Coupling Fault Models*, Accessed: July 11, 2024 [Online]. Available: https://drive.google.com/drive/folders/1C1FzvLVvXg9KDAc6wpcMtplcUIOijprM?usp=drive_link.

[20] K. L. CHENG, M. F. TSAI and C. W. WU, *Neighborhood pattern-sensitive fault testing and diagnostics for random-access memories*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **21**(11), 2002, pp. 1328–1336.

[21] C. HUZUM and P. CAŞCAVAL, *A Multibackground March Test for Static Neighborhood Pattern-Sensitive Faults in Random-Access Memories*, Electronics and Electrical Engineering (Elektronika ir Elektrotechnika) – Section System Engineering, Computer Technology **119**(3), 2012, pp. 81–86.

[22] I. MROZEK, *Multi-run Memory Tests for Pattern Sensitive Faults*, Springer, Cham, 2019.

[23] K. L. V. RAMANA KUMARI, M. ASHA RANI and N. BALAJI, *3-Cell Neighborhood Pattern Sensitive Fault Testing in Memories Using Hamiltonian and Gray Sequences*, Journal of Computational and Theoretical Nanoscience **18**(3), 2021, pp. 879–884.

[24] I. MROZEK, *Analysis of multibackground memory testing techniques*, International Journal of Applied Mathematics and Computer Science **20**(1), 2010, pp. 191–205.

[25] I. MROZEK and V. N. YARMOLIK, *Pseudo-Exhaustive Random-Access Memory Testing Based on March Tests with Random Background Variation*, Proceedings of 2018 IEEE East-West Design and Test Symposium, 2018, Kazan, Russia, pp. 510–517.