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An Improved I/O Pin for Serial Communication Interfaces

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Abstract. Modern mid-speed serial communication interfaces are required to operate in a wide range of power supply voltages, while achieving transmission rates in the order of Mbps or tens of Mbps. An important factor in determining the maximum bit rate is the I/O of the interface. An I/O pin with an improved digital push-pull output buffer is designed and implemented in a 0.18μm CMOS EEPROM process. The pin acts as an interface between an internal low voltage and an external, higher level voltage. The circuit can operate at power supply voltages from 1.6V to 5.6V and can be used in an I^{2}C UFm interface at 5 Mbps and an SPI interface at 10 Mbps. These performances were achieved through topology changes to a classic digital output buffer.

Key-words: Serial communication interface, wide voltage range, high data rate, I/O pin, digital output buffer, push pull stage.

1. Introduction

Signal and power integrity are crucial in Very Large Scale Integration (VLSI) systems. Modern trends in deep sub-micron circuit design, such as high operating frequencies, short rise/fall delays and a wide range of supply voltages, are some of the most desired targets to achieve [1–2].

Certain smart sensors, microprocessors and converters contain multiple integrated circuits which communicate with one another via serial communication buses. Many different types of serial protocols are used today to provide communications between data processing devices, like I^{2}C (Inter-Integrated Circuit) and SPI (Serial Peripheral Interface) [3].

The I^{2}C communication protocol is a well-established standard for serial data transmission between digital/mixed-signal integrated circuits in a system [4]. This protocol has multiple types

of operation, most of which (Standard, Fast, Fast+ and High Speed) are based on an open drain bus. The protocol can also operate in the Ultra Fast-mode (UFm) mode, which uses a 2-wire push pull serial bus operating at 5MHz.

A new successor to the I^2C interface, I^3C (Improved I^2C), is under development, being backward compatible with I^2C, but being able to operate at higher frequencies, up to 12.5MHz [5]. Furthermore, the I^3C specifications define an interface that can support multiple modes of communication, including high-speed and low-speed modes [6–7].

The SPI protocol is a single-ended serial interface designed for communication between integrated circuits [8]. Standard SPI is a mid-speed, full-duplex and synchronous push-pull communication bus, with operating frequencies up to 20 MHz [9–11].

The I/O pins (input buffer and output buffer) have an important role in determining the maximum of the bit rate for the serial communication interface. Those types of circuits are very popular for digital communication lines because of their high stability and large drive capability. Furthermore, I/O pins are required to switch as fast as possible, in order to be able to operate at high data transmission rates.

One important function of an I/O pin is to shift from one voltage level to another quickly [12]. Certain low power devices often employ circuitry which runs on two or more different voltage levels. For instance, ICs utilized within such requirement may run internal circuitry at a lower level voltage, while being required to interface with other circuits at higher voltages [13]. Thus, input and output buffers are required between the internal circuitry and external signals.

Output buffers can be designed as an open drain or as a push pull stage. The advantage of using the open drain configuration is the wired AND/OR capability, but the disadvantages are a slow rise (AND) /fall (OR) time and the usage of an external resistor. On the other hand, the push pull configuration offers high speed response and the capability to source or sink current [14].

This paper presents the implementation of an improved I/O pin based on a push pull output buffer topology in a 0.18μm CMOS EEPROM process with low and high voltage (20V) transistors. The I/O pin can operate for a wide range of power supply voltages, 1.6V to 5.6V. The proposed I/O pin is tested in an I^2C UFm interface operating at 5Mpbs and in an SPI interface working at 10Mbps. Furthermore, the improved I/O pin could be used in an I^3C interface, where data is transmitted with 12.5Mbps [5–7].

2. System with Digital Communication Bus

A modern electronic system such as a computer or a mobile phone contains multiple integrated circuits which communicate with one another via serial communication buses [3]. The ICs connected to such a digital bus may operate as master devices (*i.e.* can send instructions to other devices on the bus) or slave devices. The block schematic of a possible system with a communication bus is depicted in Fig. 1.

The system from Fig. 1 comprises a single master device (the microprocessor) and multiple slaves (digital or mixed-signal ICs). All the ICs are powered from the same supply voltage V_{DD} and communication on the bus takes place with logic levels associated to 0V and V_{DD}.

The power supply voltage V_{DD} could be as low as 1V, but also as high as 5.5V. However, operation at voltages below 1.7...1.8V requires using low voltage transistors, which makes operation at higher voltages, such as 5.5V, unfeasible. Thus, for the proposed I/O pin a voltage range of 1.6V...5.6V (achievable with high voltage transistors) is considered, which is sufficient for ICs that aren't specifically designed for very low voltage operation.

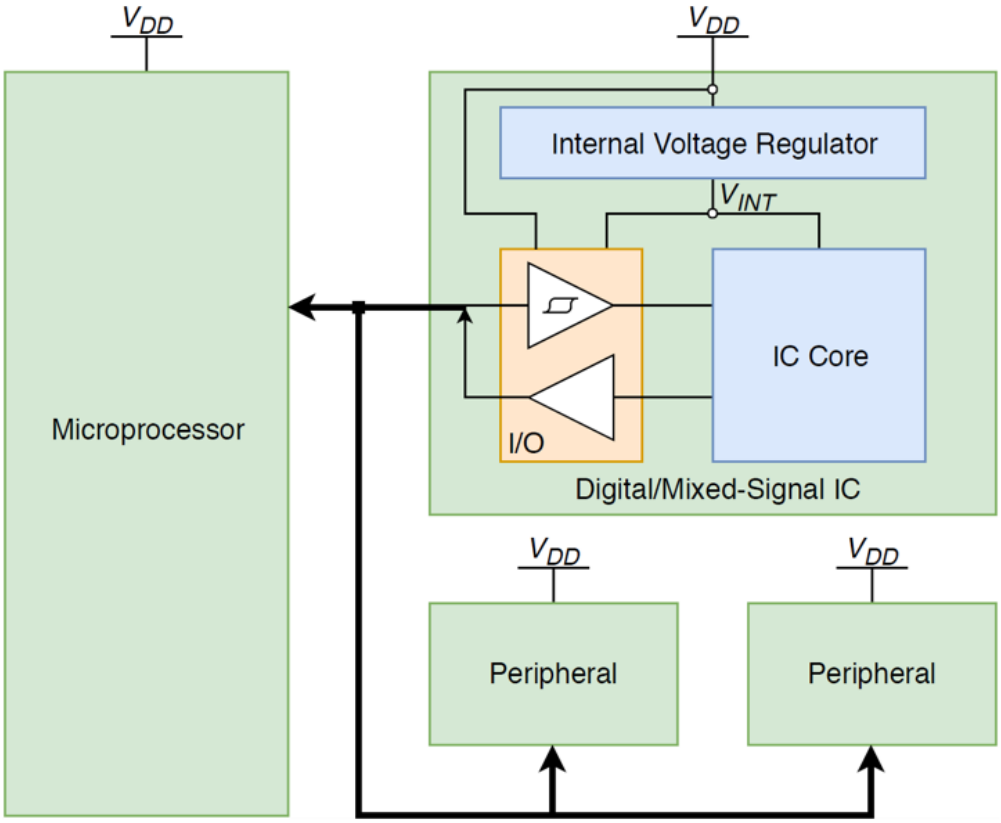

Fig. 1. System with Digital Communication Bus.

Operating the IC core at voltages greater than 2V is inefficient from a power consumption point of view. Therefore, most modern digital and mixed-signal ICs have an internal voltage regulator which generates the supply voltage for the core, $V_{INT} \leq V_{DD}$. Thus, there is a need for an I/O pin circuit which interfaces between the external bus (powered by V_{DD}) and the IC core.

In this paper, communication protocols with clock and data signals are considered. For such protocols, the clock signal is generated by the master and is used to synchronize the data that is communicated on the bus. When the master sends data to a slave (write operation), there is no problem establishing a clear timing relationship between the clock and data signals. However, when the master is receiving data from a slave (read operation), a significant delay may arise. The clock is processed by an input buffer and sent to the IC core, which shifts out next data bit and passes it to the bus through an output buffer.

The parameter describing the delay during the read operation is typically called access time (or data valid time, $t_{VD,DAT}$) and is defined as the time difference between one of the clock edges and the moment when the next data value is available on the bus [15–19]. For protocols operating at MHz frequencies, the access time is mainly determined by the delays of the input and output buffers. Thus, in processes with slow high voltage (HV) transistors used for pad periphery, standard buffer topologies may no longer be adequate.

3. I/O Pin

3.1. Input Buffer

The schematic of the input buffer is shown in Fig. 2. The buffer has a high voltage (HV) side, powered by the supply voltage (V_{DD}), and a low voltage (LV) part, supplied from the internal voltage V_{INT}.

The high voltage part is represented by a latch-based Schmitt trigger [20], comprising three inverter stages built with HV transistors (P_{HV1}, N_{HV1}), (P_{HV2}, N_{HV2}) and (P_{HV3}, N_{HV3}). The circuit's hysteresis ensures a good reception of the digital signal from the communication bus (connected to its input *IN*), reducing the chance of unwanted multiple transitions which could be caused by noise. This trigger topology was preferred due to its good dynamic performance (improved speed compared to the standard CMOS trigger [21]).

The output signal of the trigger (OUT_T) is translated into low voltage using an inverter built with HV transistors (P_{HV4}, N_{HV4}) which is powered from the internal low voltage V_{INT}. However, due to the HV devices being slow at low voltages, this inverter has poor switching performance. Thus, in order to regenerate the edges of the output LV signal (*OUT*) a faster low voltage inverter (P_{LV1}, N_{LV1}) is added.

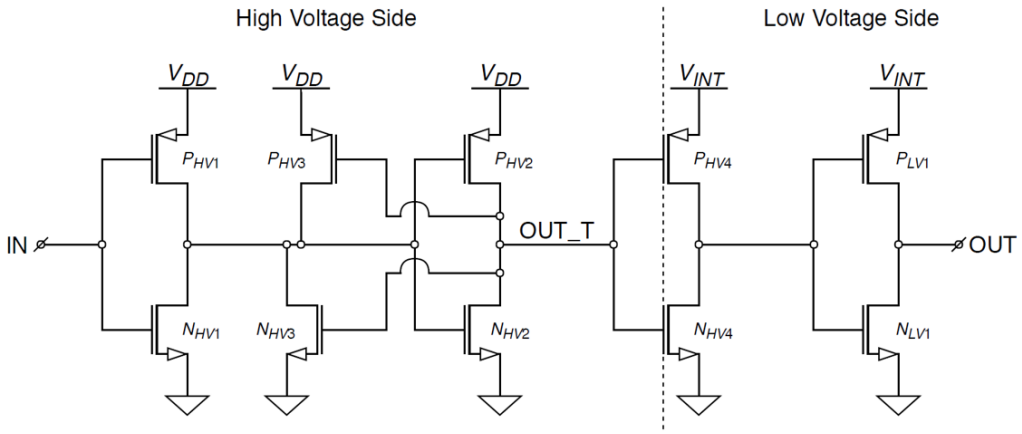

Fig. 2. Input buffer schematic.

The input buffer circuit was implemented in the 0.18um process and sized for minimum delay, as well as allowing for operation with input logic levels V_{IL} = 30% V_{DD} (logic "0") and V_{IH} = 70% V_{DD} (logic "1") for V_{DD} = 1.6...5.6 V. Its operation was tested through HSPICE simulations, resulting in the waveforms from Figs. 3, 4 for the V_{DD} = 1.6V and V_{DD} = 5.6V, respectively. A good agreement between the simulation results and the expected waveforms is observed.

For $V_{INT} < 1.9$V (Fig. 3), the LV and HV supply voltages are equal ($V_{DD} = V_{INT}$). Therefore at 1.6V, both the *OUT_* T and the *OUT* signals have the same logic "1" level (*i.e.* there is no level shifting). At 5.6V, however the HV inverter (P_{HV4}, N_{HV4}) powered from V_{INT} shifts the output of the trigger into LV and the *OUT* and OUT_T signals have different logic "1" levels.

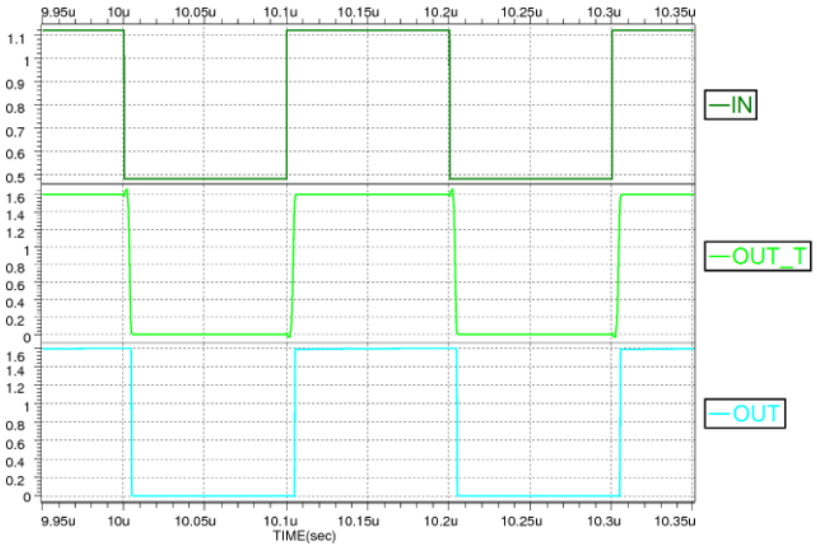

Fig. 3. Input buffer waveforms for V_{DD} = 1.6V.

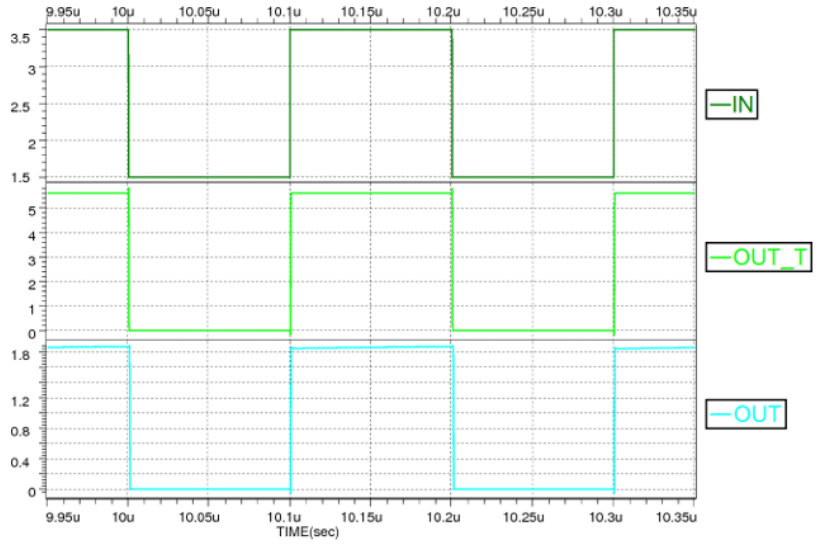

Fig. 4. Input buffer waveforms for V_{DD} = 5.6V.

On the waveforms from Figs. 3, 4, the following timing parameters were obtained: t_r – *OUT* signal rising time (10% to 90% of V_{DD}), t_f – *OUT* signal falling time, t_{plh} – propagation delay of low to high transition from *IN* to *OUT* (50% of V_{INT} to 50% of V_{DD}), and t_{plh} - high to low propagation delay. The average value of the current consumed by the HV side (powered by V_{DD}) was also determined. The variation with temperature (from –40°C to 125°C) and process corner was investigated for both V_{DD} voltages and the results are given in Table 1.

Table 1. Input buffer dynamic parameters

Parameter	Power Supply	Value		
		Min	Typ	Max
t_r [ns]	1.6V	0.25	0.27	0.39
	5.6V	0.13	0.14	0.30
t_f [ns]	1.6V	0.28	0.32	0.39
	5.6V	0.16	0.22	0.24
t_{plh} [ns]	1.6V	3.27	6.56	14.4
	5.6V	0.37	0.52	0.73
t_{plh} [ns]	1.6V	3.16	5.35	11.10
	5.6V	0.64	0.78	0.96
avg (i_{DD})	1.6V	0.022	0.023	0.042
@5MHz [mA]	5.6V	5.26	5.85	6.19

The rise and fall times are very small for both supply voltages V_{DD} = 1.6 V and V_{DD} = 5.6 V, due to the fact the *OUT* signal is generated by the fast LV inverter (P_{LV1}, N_{LV1}). The maximum propagation delay at low supply voltages is $\sim$ 14% of the bit time at 10Mbps, as a result of the HV transistors being slow at low supply voltages. The current consumption is large when operating at 5.6V due to the fact that the input signal has logic levels 30% V_{DD} and 70% V_{DD} (*i.e.* worst case operation in most modern communication protocols).

3.2. The Standard Output Buffer Circuit

The schematic of a standard output buffer topology is given in Fig. 5. The low voltage side receives the input data signal (*IN*), which is gated with the enable signal *EN*. The level shifters allow the change of the gated signals logic "1" level, providing high voltage outputs (P_HV, N_HV). The buffer also has an enable control signal (*EN*), which, when low, indicates that neither transistor should be driving the output (high output impedance – hiZ).

The Non-overlap Logic block is driven by the level shifters and generates the P_G and N_G signals which have a "break-before-make" non-overlap. This has an important role for cross current and ground bounce issues [22].

A buffer of the type shown in Fig. 5 was designed and implemented in a 0.18μm CMOS EEPROM process. Its operation was tested through HSPICE simulations, with the resulting waveforms shown in Figs. 6, 7, for external (and power supply) voltages V_{DD}=1.6V and V_{DD}=5.6V, respectively. In the simulations, a capacitive load of 30pF was considered. In both cases, the data (*IN*) is transmitted at a speed of 10Mbps, which corresponds to an input signal with a switching frequency of 5 MHz.

The operation of the level shifters can be observed in Fig. 4, where V_{DD} = 5.6V is higher than the internal voltage $V_{INT} \approx$ 1.9 V. The LV input is changed into HV signals (P_HV and N_HV). For $V_{INT} <$ 1.9V (Fig. 6), the LV and HV supply voltages are equal ($V_{DD} = V_{INT}$). Thus, the level shifters no longer change the voltage level, but only contribute to the buffer delay (especially due to their high output rise time). This is one of the limitations of this topology.

The logic "1" pulse is wider for P_G than N_G (as seen in Figs. 6, 7), which means the output transistors never conduct at the same time ("break-before-make"). Due to the reduced speed of the high voltage (20V) transistors available in the process, the Non-overlap Logic block introduces an unnecessarily large delay when operating at low voltages (V_{DD} = 1.6V – Fig. 3), increasing overall delay. This is another disadvantage of the basic topology from Fig. 5.

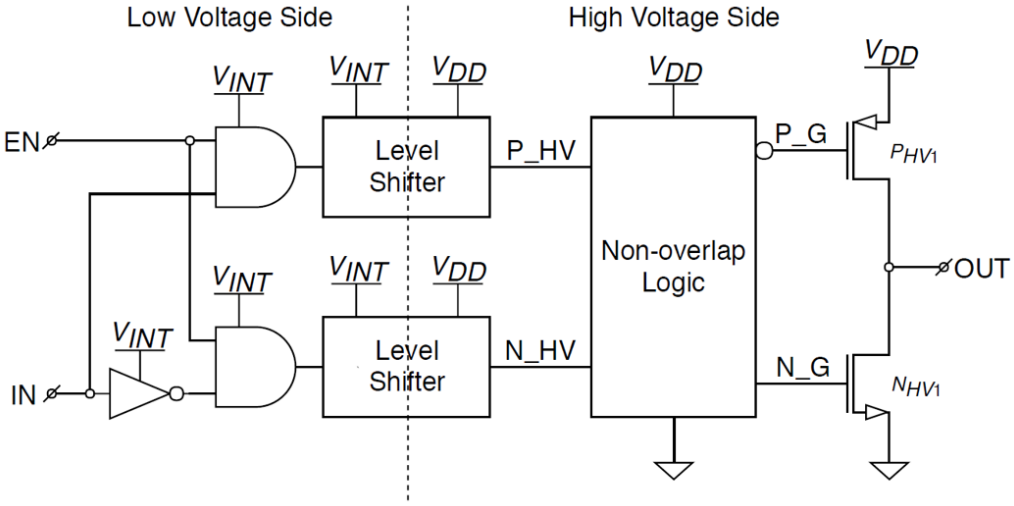

Fig. 5. Standard output buffer schematic.

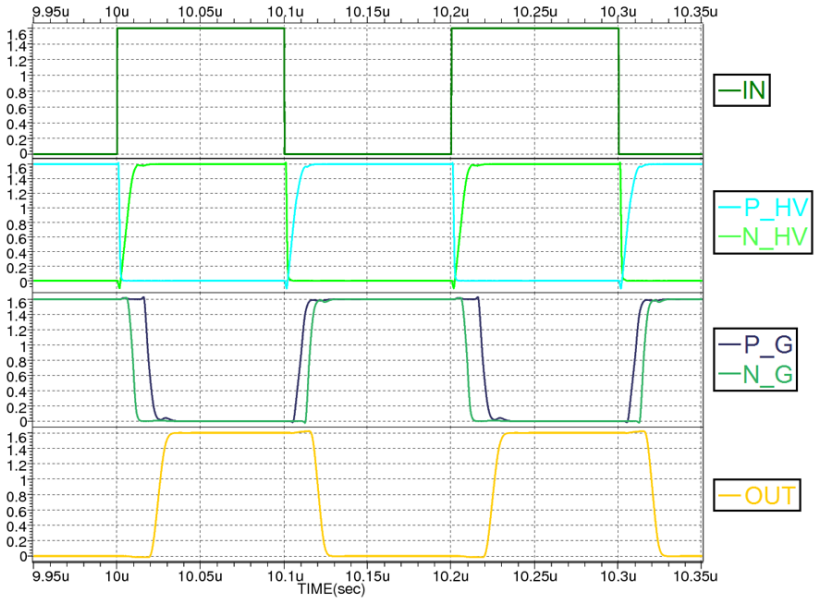

Fig. 6. Standard digital output buffer waveforms for V_{DD} = 1.6V.

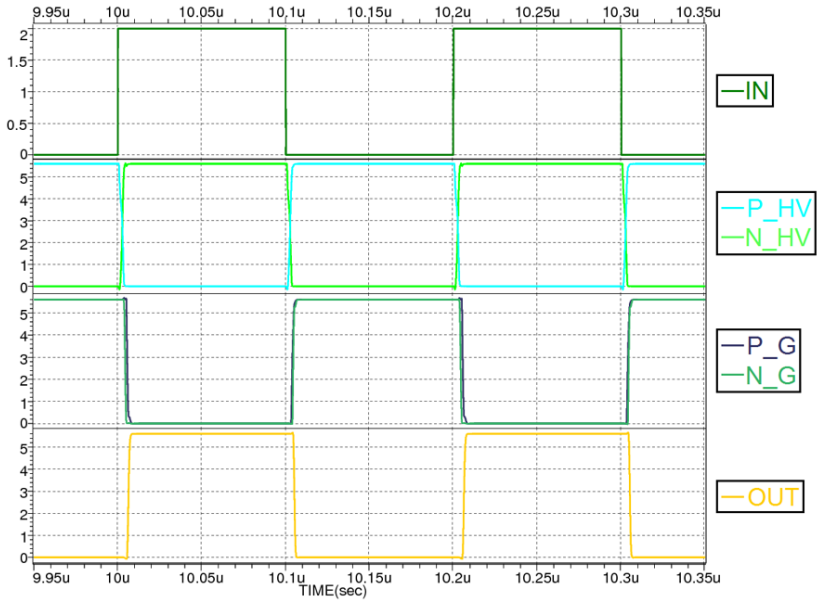

Fig. 7. Standard digital output buffer waveforms for V_{DD} = 5.6V.

Table 2 shows the dynamic parameters of the standard buffer and their spread with temperature and process corner. Furthermore, the main contributors to the propagation delay were extracted: t_{d_nmos} – output n-MOS N_{HV1} turn-on delay (N_G rising edge at 50% of V_{DD} to *OUT* falling edge at 50% of V_{DD}), t_{d_pmos} – output p-MOS P_{HV1} turn-on delay (P_G falling edge at 50% of V_{DD} to *OUT* rising edge at 50% of V_{DD}), t_{nov_r} – non-overlap dead time for low to high transition (N_G falling edge at 50% of V_{DD} to P_G falling edge at 50% of V_{DD}), and t_{nov_f} - non-overlap dead time for high to low transition (P_G rising edge at 50% of V_{DD} to N_G rising edge at 50% of V_{DD}).

Acceptable rise and fall times and propagation delays are obtained for V_{DD} = 5.6 V. In contrast, at 1.6 V, the rising and falling times are up to ∼6 times as large, while the propagation delays are up to ∼4 times greater. This propagation delay is as high as ∼30% of the bit time at 10Mbps. This can be an issue especially for two-wire communication (clock and data), where the data being sent has to switch within a certain time from an input clock edge. As can be seen in Table 2, the main contributors to the propagation delays are the turn-on times of the output transistors (for example, at 1.6V, the n-MOS delay is more than half of the overall high to low propagation delay). Furthermore, the non-overlap dead times have a significant impact on the buffer delay at 1.6V, while being very small at 5.6V (also a disadvantage since cross-conduction may appear).

Table 2. Basic output buffer dynamic parameters

Parameter	Power Supply	Value		
		Min	Typ	Max
t_r [ns]	1.6V	6.2	8.0	9.3
	5.6V	1.2	1.4	1.8
t_f [ns]	1.6V	5.2	6.7	7.5
	5.6V	0.9	1.2	1.5
t_{plh} [ns]	1.6V	19.8	25.5	28.1
	5.6V	5.5	6.7	7.5
t_{phl} [ns]	1.6V	16.8	20.8	24.8
	5.6V	4.4	5.9	5.9
t_{d_nmos} [ns]	1.6V	9.8	11.6	13.9
	5.6V	0.96	0.98	1.07
t_{d_pmos} [ns]	1.6V	5.3	5.9	7.0
	5.6V	0.6	1.2	1.6
t_{nov_r} [ns]	1.6V	8.4	9.2	12.3
	5.6V	1.14	1.2	1.6
t_{nov_f} [ns]	1.6V	4.3	5.2	6.9
	5.6V	0.5	0.6	0.7
avg (i_{DD})	1.6V	0.342	0.347	0.356
@5MHz [mA]	5.6V	1.26	1.28	1.31

3.3. The Improved Output Buffer Circuit

In order to deal with the limitations described in the previous section, improvements were made to the standard topology from Fig. 5. The proposed output buffer is shown in Fig. 8.

A significantly lower propagation delay from *IN* to *OUT* is obtained, as demonstrated by simulation from Figs. 9, 10, for V_{DD} = 1.6V and 5.6V, respectively, and an output load of C_L=30 pF. For these simulations, a bit-rate of 20 Mbps was considered, equivalent to a switching frequency of 10 MHz, in order to illustrate the increased speed of the proposed buffer.

The buffer's delay was reduced through several changes. A faster n-MOS transistor, with a lower threshold voltage, was available in the used process. This transistor was used instead for the N_{HV1} device from Fig. 5. The threshold of N_{HV1} is low enough that it can be driven with a LV signal. In this manner, the level shifter for the n-MOS, a significant delay contributor, was eliminated. In addition, the delay is further reduced, due to the removal of all HV devices from the n-MOS drive path.

The level shifter is still necessary for P_{HV1}, since its gate needs to be driven with V_{DD} in order for it to be OFF. This transistor is driven by the P_{HV2}, N_{HV2} stage. The effect of the level shifter delay was diminished by using as N_{HV2} the low threshold n-MOS (same as N_{HV1}) and driving its gate with a LV signal (N_D). Thus, the level shifter's slow rising slope no longer has any contribution to P_{HV1} turn-on delay. This improvement can be seen in Fig. 9, where P_G falls very quickly.

A small rising delay was added for the N_D signal. This delay block was sized so that its output signal N_D rises while P_D is halfway through switching, so P_{HV2} is basically OFF (due to its high threshold voltage) when N_{HV2} turns ON. This non-overlap is also maintained at 5.6V, as can be seen in Fig. 10.

The effect of the non-overlap delay was reduced through the fact that P_{HV1} turning ON is not conditioned by N_{HV1} turning OFF. This is permissible since N_{HV1} switches faster than

P_{HV1}. N_{HV1} turn ON conditioning is done with the N_EN signal, which is obtained by shifting P_D back to LV. In this way, the propagation delay was reduced, while maintaining the previous "break-before-make" non-overlap (P_G, N_G signals – Figs. 9, 10).

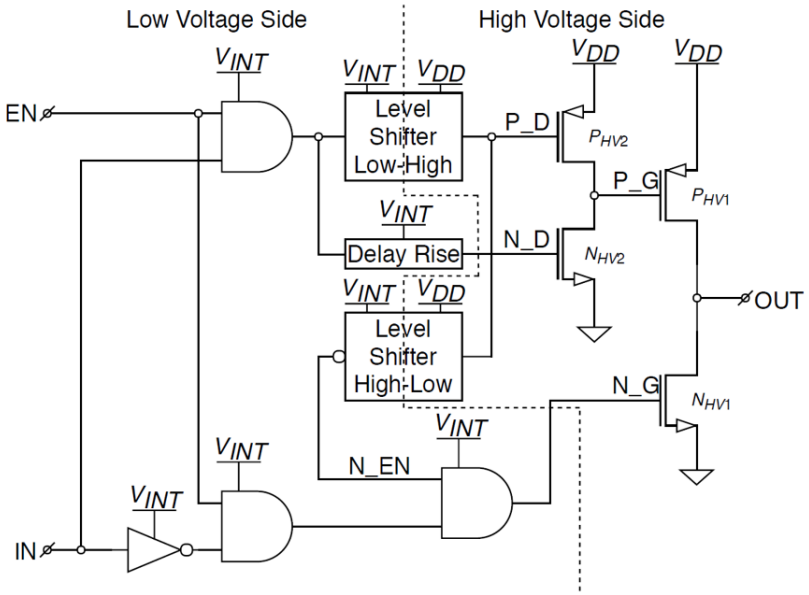

Fig. 8. Improved output buffer schematic.

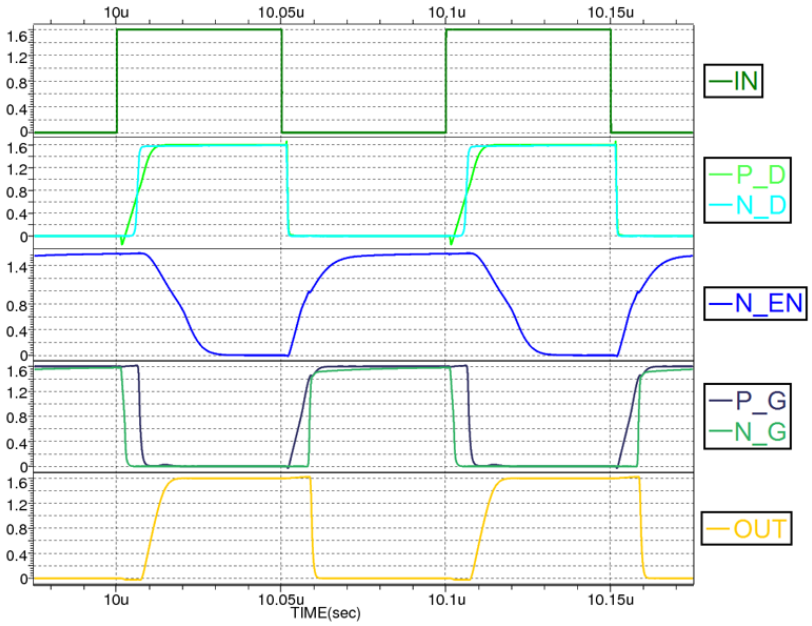

Fig. 9. Improved buffer waveforms for V_{DD} = 1.6V.

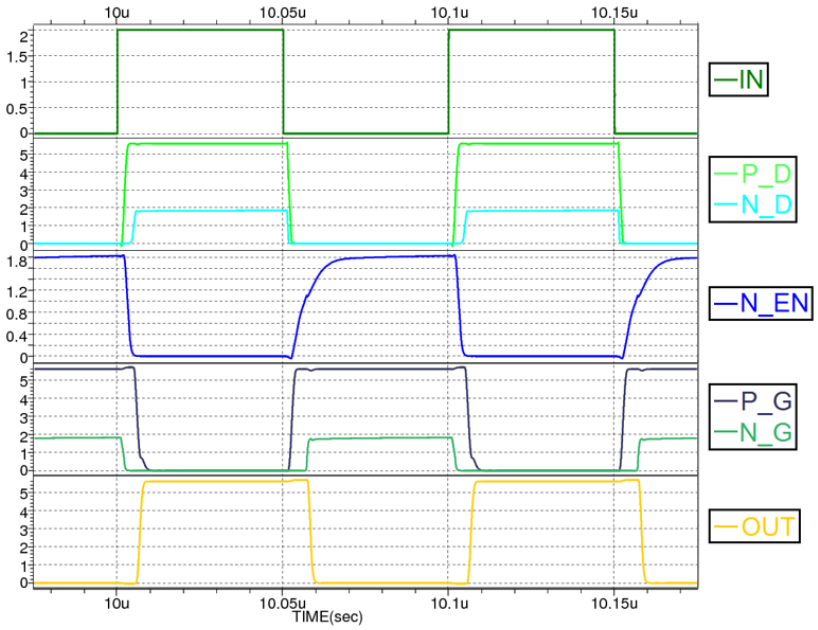

Fig. 10. Improved buffer waveforms for V_{DD} = 5.6V.

The dynamic parameters of the improved buffer and their spread with temperature and process corner is shown in Table 3. In this case, the contributors to the propagation delay are redefined as: t_{d_nmos} – output n-MOS N_{HV1} turn-on delay (N_G rising edge at 50% of V_{INT} to OUT falling edge at 50% of V_{DD}), t_{d_nmos} – output p-MOS P_{HV1} turn-on delay (P_G falling edge at 50% of V_{DD} to OUT rising edge at 50% of V_{DD}), t_{nov_r} – non-overlap dead time for low to high transition (N_G falling edge at 50% of V_{INT} to P_G falling edge at 50% of V_{DD}), and t_{nov_f} - non-overlap dead time for high to low transition (P_G rising edge at 50% of V_{DD} to N_G rising edge at 50% of V_{INT}).

The faster n-MOS output transistor has a $\sim$40% lower turn-on time (compared to the standard HV transistor) and produces a fall time at 1.6V that is up to 5 times lower than the values from Table 2. The rise time is also improved $\sim$1.3 times and the output p-MOS turn-on delay is $\sim$1.5 times lower, due to P_G switching faster (because N_{HV2} is faster). However, the improvement for pull up is not as significant as for the pull down, due to the p-MOS having a small overdrive at 1.6V (because of its higher threshold voltage).

The non-overlap times at 1.6V are reduced by up to $\sim$50%. Moreover, these dead times have a reduced variation with power supply, ensuring that the non-overlap still exists at 5.6V (4–5ns for the improved buffer compared to $<$ 2ns for the standard one).

The most significant improvement, however, is the decrease of the propagation delay at 1.6V, resulting in a buffer that is twice as fast as the previous implementation. This, in turn allows it to operate at twice as high bit-rates (20 Mbps vs. the original 10 Mbps).

Table 3. Improved output buffer dynamic parameters

Parameter	**Power Supply**	**Value**		
		Min	**Typ**	**Max**
t_r [ns]	1.6V	5.7	6.7	8.6
	5.6V	1.4	1.6	1.9
t_f [ns]	1.6V	1	1.2	1.4
	5.6V	1.2	1.4	1.8
t_{plh} [ns]	1.6V	8.9	11.0	14.2
	5.6V	5.6	6.7	8.5
t_{phl} [ns]	1.6V	6.9	9.0	12.5
	5.6V	6.2	7.7	10.5
t_{d_nmos} [ns]	1.6V	6.4	6.7	7.1
	5.6V	4.5	4.9	5.6
t_{d_pmos} [ns]	1.6V	3.7	4.0	4.7
	5.6V	0.7	0.77	0.97
t_{nov_r} [ns]	1.6V	4.0	4.6	5.8
	5.6V	3.9	4.2	5.1
t_{nov_f} [ns]	1.6V	2.6	3.1	3.2
	5.6V	4.7	4.9	5.5
avg (i_{DD})	1.6V	0.295	0.297	0.303
@5MHz [mA]	5.6V	1.027	1.031	1.036

Compared to the basic circuit, the current drawn from V_{DD} by the improved buffer (at 5MHz) is reduced by $\sim$15..20%. This is due to the simplified drive of the output n-MOS, powered by the LV supply, V_{INT}.

A DC analysis of the improved output buffer was carried out and the results are given in Table 4. The output transistors P_{HV1}, N_{HV1} were designed to allow for current loads I_{OL} = – 3 mA and I_{OH} = 3 mA for power supply voltages V_{DD} = 1.6...5.6V.

Table 4. DC parameters for output buffer

Parameter	Power Supply	Value		
		Min	Typ	Max
V_{OL} [mV] @	1.6V	85.5	100	140
I_{OL} = – 3mA	5.6V	14.4	18.5	25.7
V_{OH} [V] @	1.6V	1.43	1.47	1.50
I_{OH} = 3mA	5.6V	5.56	5.57	5.58

In Table 4, fairly low values for V_{OL} and fairly high ones for V_{OH} can be seen, which show that the buffer has a high current drive capability. However, the increased size of the output transistors means that they also have higher capacitances, which raises delay (hence the need for a faster topology).

In order to better compare the operation of the two topologies across the entire supply voltage range (V_{DD} = 1.6V...5.6V), their maximum propagation delays were represented in Fig. 11 (for low-high transition) and in Fig. 12 (for high-low transition), with a capacitive load of 30 pF. The main objective of fast operation at low voltages is achieved, since the improved buffer is roughly twice as fast for $V_{DD} < 2$ V. Furthermore, the delays of the improved buffer have a smaller variation, due to the fact that most driving logic was switched into the low voltage side (V_{INT}

is limited at ∼1.9V). Even if the standard topology performs better at higher V_{DD} values, this reduced variation is an advantage of the improved topology (the delay is more stable with respect to power supply).

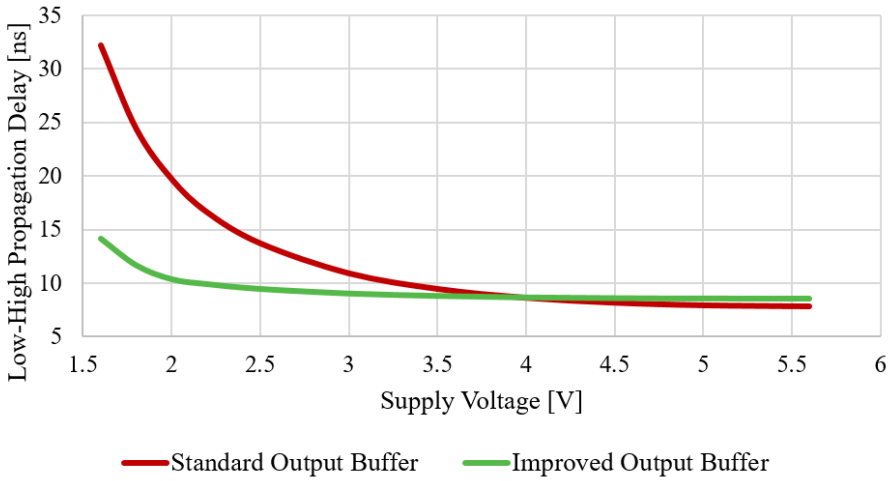

Fig. 11. Low-High Propagation Delay vs. Supply Voltage for the two buffer topologies.

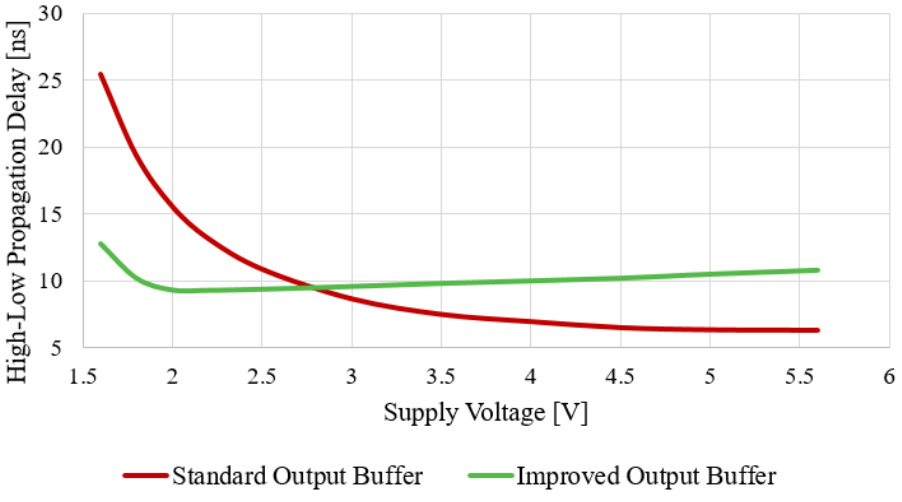

Fig. 12. High-Low Propagation Delay vs. Supply Voltage for the two buffer topologies.

4. Application of the Improved I/O Pin in Digital Communication Interfaces

4.1. I²C Ultra-Fast Mode Interface

Communication using the I²C Ultra-Fast Mode protocol involves two signals: a 5 MHz clock (*USCL*) and data (*USDA*). For a digital/mixed-signal IC operating as a slave, the communication interface is depicted in Fig. 13.

Due to the fact that a slave device only receives the clock signal and has no impact on its generation, the *USCL* pin only has an input buffer connected to it. For the data pin, both an input and an output buffer are used, since the slave device needs to be able to receive as well as send data, depending on the master's request. In order to generate the internal *DATAIN* and *CLOCKIN* signals, processing paths are used, which could allow for the gating of these signals based on one or more *DCTRL* or *CCTRL* control signals (depending on what is required by the operation of the circuit), as well as suppressing spikes of less than 10 ns [4].

In the I²C protocol, the data being transmitted is grouped into bytes and is serialized. Therefore, an 8-bit shift register is required in order to convert the information from the internal multiple bit bus (*DATAREAD*) into a single data signal (*DATAOUT*) – or vice-versa. Data is loaded into the register every 9 clock periods (1 byte + 1 acknowledge bit [4]), when the signal *LOAD* is generated. In Fig. 11, this register is only shown in a configuration for sending data (*i.e.* a read operation), since this is the situation in which the delays of the input and output buffers are critical.

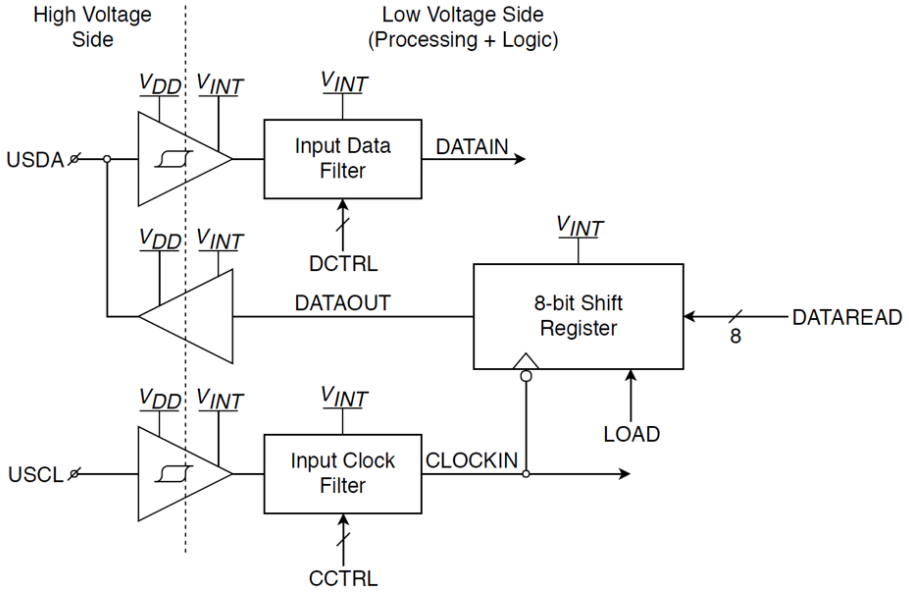

Fig. 13. Block schematic of the I²C UFm interface.

The I²C UFm interface was implemented in the 0.18μm CMOS EEPROM process. Its operation when sending data (read) was investigated through HSPICE simulations performed for

V_{DD} = 1.6V and for V_{DD} = 5.6V with a capacitive load on *USDA* C_L = 50 pF, using both the standard output buffer and the improved one (Figs. 14, 15). Only the *USDA* signal is represented separately for each case, since the rest of the interface is identical for both cases. The operating clock frequency for the I^{2}C UFm is 5 MHz [4], equivalent to a data transmission rate of 5 Mbps.

The sequencing of the interface signals can be observed in Figs. 14, 15: internal *CLOCKIN* signal is generated from *USCL* and data (*DATAOUT*) is shifted on its falling edge. The output buffer then drives the *USDA* line based on the value of *DATAOUT*. It should be noted that when data is being sent by the slave, the master must release the *USDA* output, so that no conflict appears.

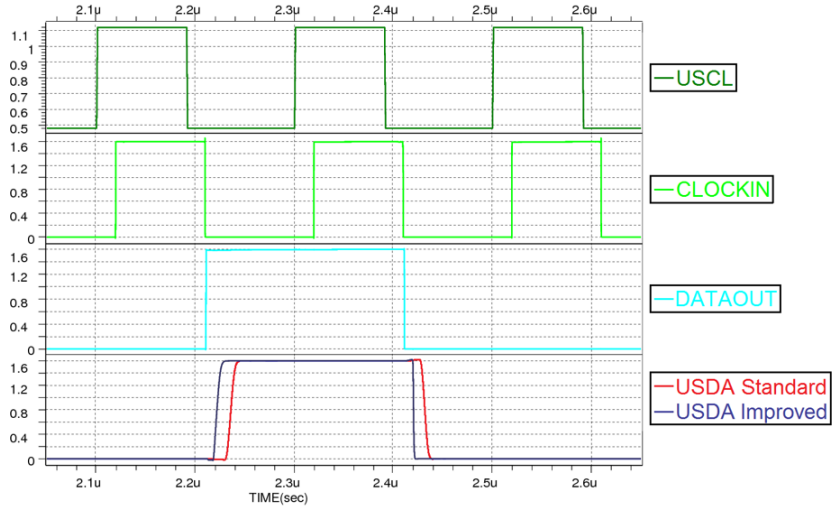

Fig. 14. I^{2}C UFm interface operation at 1.6V with the standard and improved output buffers.

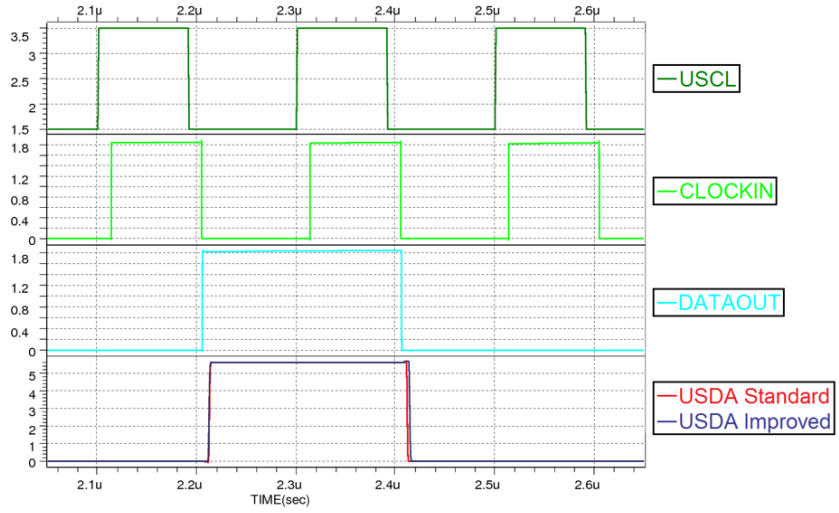

Fig. 15. I^{2}C UFm interface timing operation 5.6V with the standard and improved output buffers.

On the waveforms from Figs. 14, 15, the following data hold times [4] were measured: t_{HD,DAT_LH} (delay time from *USCL* falling edge reaching 30% V_{DD} to *USDA* rising edge reaching 30% V_{DD}), t_{HD,DAT_HL} (delay time from *USCL* falling edge reaching 30% V_{DD} to *USDA* falling edge reaching 70% V_{DD}). Essentially, the data hold time represents the delay from the ending of a falling clock edge to the start of a data transition (rising or falling).

The data valid times (read access times) [4] were also measured: t_{VD,DAT_LH} (delay time from *USCL* falling edge reaching 30% V_{DD} to *USDA* rising edge reaching 70% V_{DD}), t_{VD,DAT_HL} (delay time from *USCL* falling edge reaching 30% V_{DD} to *USDA* falling edge reaching 30% V_{DD}). The data valid time represents the delay from the ending of a falling clock edge to the ending of a data transition.

The values of the four timing parameters are given in Table 5, for the case when the standard buffer is used, and Table 6, for the case with the improved buffer. These values are mostly influenced by the delays of the suppression filters, the input *USCL* buffer and the output *USDA* buffer (the low voltage logic has negligible delay – as seen in Fig. 13). Of these two, the most significant contributor is the output buffer, as shown by the fact that using the proposed buffer reduces access time by up to ∼20ns (Table 5 vs. Table 6).

Table 5. I^{2}C UFm interface dynamic parameters with the standard output buffer

Parameter	**Power Supply**	**Value**		
		f_{USCL} **= 5 MHz**		
		Min	**Typ**	**Max**
t_{HD,DAT_LH}	1.6V	35.9	45.5	59.4
	5.6V	16.6	19.9	22.8
t_{HD,DAT_HL}	1.6V	32.5	39.3	52.9
	5.6V	15.9	19	22.3
t_{VD,DAT_LH}	1.6V	39.9	49.5	65.1
	5.6V	17.2	21	23.5
t_{VD,DAT_HL}	1.6V	33.1	39.6	53.4
	5.6V	16.4	19.8	23

Table 6. I^{2}C UFm interface dynamic parameters with the improved output buffer

Parameter	**Power Supply**	**Value**		
		f_{USCL} **= 5 MHz**		
		Min	**Typ**	**Max**
t_{HD,DAT_LH}	1.6V	24.6	31	39
	5.6V	16.7	19.9	21.1
t_{HD,DAT_HL}	1.6V	23.8	28.8	39
	5.6V	15.9	19	22.3
t_{VD,DAT_LH}	1.6V	28.6	35.5	44.7
	5.6V	17.5	19.8	21.9
t_{VD,DAT_HL}	1.6V	24.9	30.2	39.9
	5.6V	18.7	22.4	25.5

The I^{2}C UFm specification only imposes minimum values for the mentioned timing parameters and therefore both buffers can be used in such an interface. However, in some applications, the worst case access time of the interface with the old buffer (nearly 65 ns – Table 6) could be unacceptable (for instance, for the PCU9661 bus expander [23], the maximum data valid time

is 45 ns). This can be observed in Figs. 16, 17, in which the variations of the maximum access times (low-high and high-low, respectively) of the two buffers with the supply voltage are represented. These plots show that, while the interface with the improved buffer can achieve the access time imposed by PCU9661 starting from 1.6V, the one with the standard buffer could do so for $V_{DD} > 1.8$V.

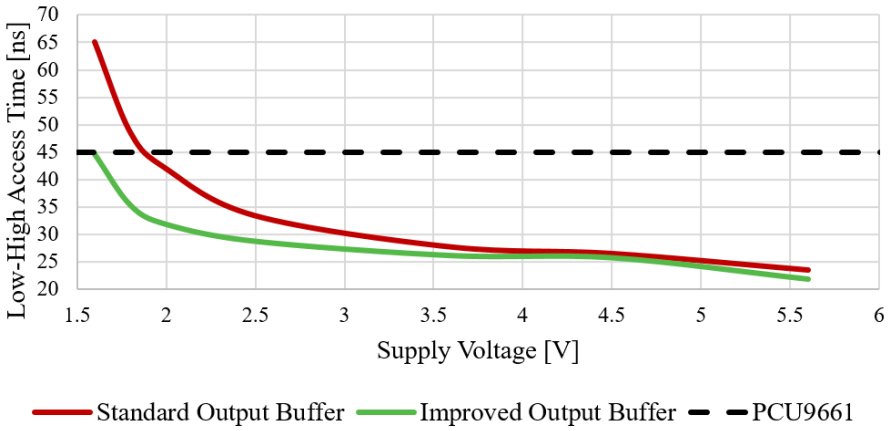

Fig. 16. I^{2}C UFm interface Low-High Access Time vs. Supply Voltage – comparison.

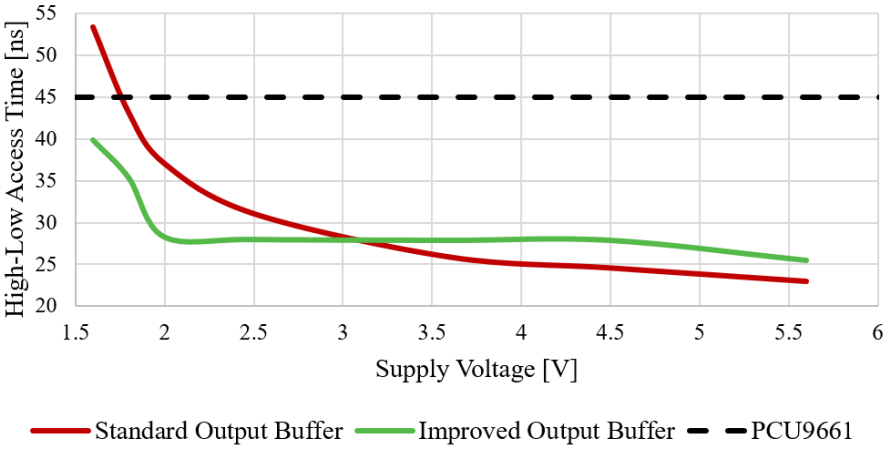

Fig. 17. I^{2}C UFm interface High-Low Access Time vs. Supply Voltage – comparison.

4.2. SPI Interface

Communication using the SPI protocol uses 4 wires for communication: clock, data input, data output and chip select, allowing for operation at several data transmission rates (similarly to I^{2}C). The two separate data lines allow for push-pull drivers without the need to take into account possible conflicts between ICs, thus leading to higher operating frequencies.

SPI has four operation modes, depending on the clock idle polarity and respectively its active edge (*i.e.* the edge which triggers the data switch). For the purpose of this paper, we will consider an interface operating in the mode (0,0), which means that the clock idles at "0" and data switches on the falling edge.

For a digital/mixed-signal IC operating as a slave, the SPI communication interface is depicted in Fig. 18. For simplicity, only the data input (*SI* – Slave Input), the data output (*SO* – Slave Output) and clock (*SCK* – Serial Clock) were illustrated. The main difference compared to the I^{2}C UFm interface from Fig. 13 consists in the separate data wires. It should also be noted that new data is loaded into the register every 8 clocks (as opposed to 9), since there is no acknowledge bit in SPI.

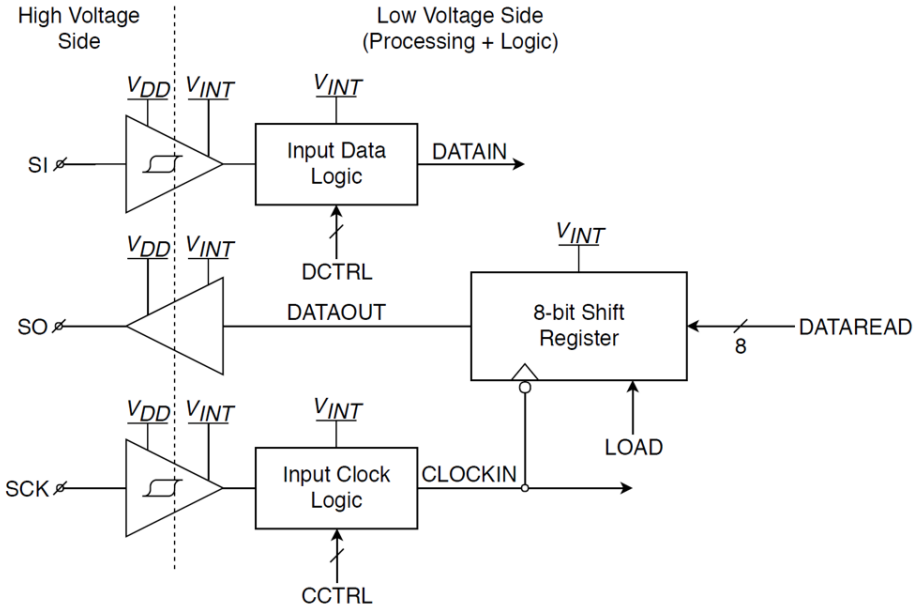

Fig. 18. Block schematic of the SPI interface.

The SPI interface was implemented in the 0.18μm CMOS EEPROM process. Its operation when sending data (read) was investigated through HSPICE simulations performed for the two supply voltages (1.6V and 5.6V) and a load on *SO* C_L = 30 pF, using both the standard output buffer and the improved one (Figs. 19, 20). An operating frequency of 10 MHz was considered.

On the waveforms from Figs. 19, 20, a behavior similar to that described for the I^{2}C UFm interface can be observed. The measured data hold and data valid times for the cases with the two output buffers are given in Table 7 and Table 8, respectively. These values are slightly lower than for the I^{2}C UFm interface and can be explained by the fact that for SPI there is no input buffer on the *SO* wire (the input buffer contributes a small capacitive load).

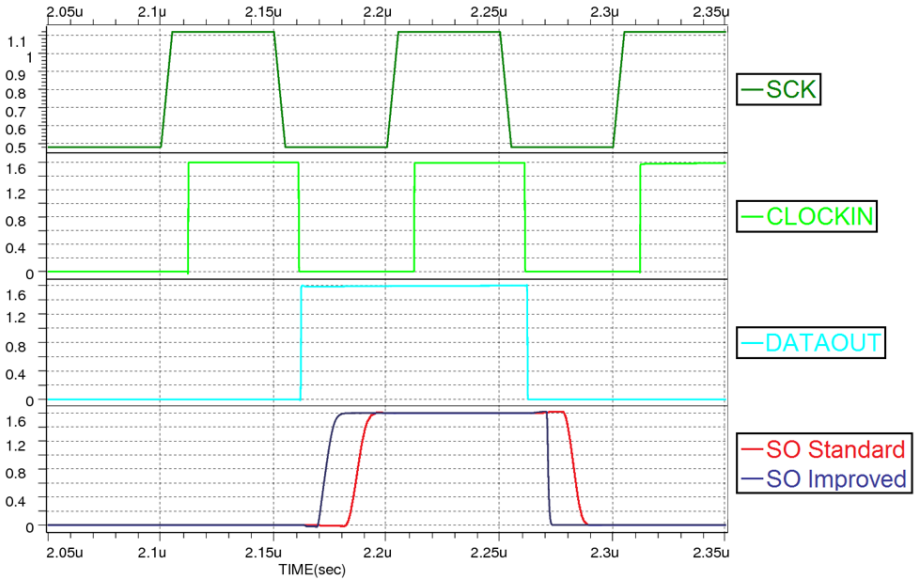

Fig. 19. SPI interface operation at 1.6V with the standard and improved output buffers.

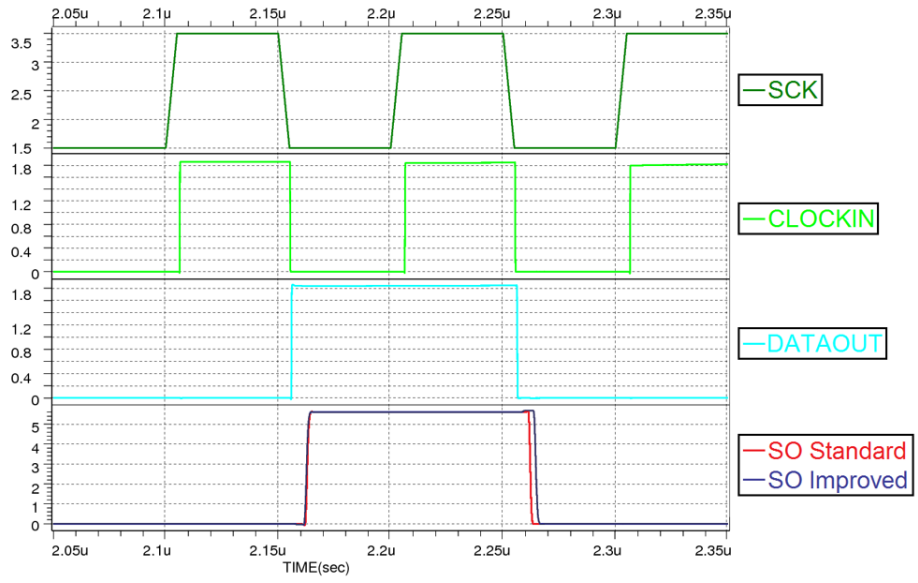

Fig. 20. SPI interface operation at 5.6V with the standard and improved output buffer.

Table 7. SPI interface dynamic parameters with the standard output buffer

Parameter	**Power Supply**	**Value**		
		f_{SCK}**= 10 MHz**		
		Min	**Typ**	**Max**
t_{HD,DAT_LH}	1.6V	23.4	30.7	43.1
	5.6V	6.8	9.0	13.1
t_{HD,DAT_HL}	1.6V	20.7	26.3	37.8
	5.6V	7.2	9.5	13.6
t_{VD,DAT_LH}	1.6V	26.3	34.0	46.9
	5.6V	6.1	8.1	11.8
t_{VD,DAT_HL}	1.6V	22.9	29.2	41.1
	5.6V	6.58	8.59	12.3

Table 8. SPI interface dynamic parameters with the improved output buffer

Parameter	**Power Supply**	**Value**		
		f_{SCK}**= 10 MHz**		
		Min	**Typ**	**Max**
t_{HD,DAT_LH}	1.6V	13	16.8	24.4
	5.6V	6.8	7.8	8.7
t_{HD,DAT_HL}	1.6V	12	15.6	24.5
	5.6V	8.0	10.7	11
t_{VD,DAT_LH}	1.6V	12.3	15.9	24.6
	5.6V	7.5	8.5	9.4
t_{VD,DAT_HL}	1.6V	12.7	16.4	25.1
	5.6V	8.5	11.3	11.7

The improved access (data valid) times from Table 8 allow for higher transmission rates at lower voltages compared to existing SPI products. The variation of these times (maximum values) with the supply voltage are represented in Figs. 21, 22, for both output buffers and for two SPI products, CAT25128 [17] and NXH5104 [18].

CAT25128 [17] has a maximum $t_{VD,DAT}$ = 40 ns for 10 Mbps, but achieves it only at voltages greater than 2.5V. On the other hand, the interface with the improved buffer has a 25.1 ns maximum access time (Table 8), which means it can operate at a clock frequency of 10 MHz starting from 1.6 V. Furthermore, for operation at 20 MHz, the datasheet of CAT25128 specifies $t_{VD,DAT}$ = 20 ns, achieved for $V_{DD} \geq 4.5$ V. With the new output buffer, this bit-rate is attainable at voltages as low as 2 V.

The circuit NXH5104 [18] has a more restrictive specification: $t_{VD,DAT}$ = 22.5 ns for operation at 10 MHz and 1.8V. This is also achievable by the interface containing the improved buffer – maximum access time at 1.8 V is 15.8 ns. Using the standard buffer, however, this can only be fulfilled for $V_{DD} \geq 2.5$ V.

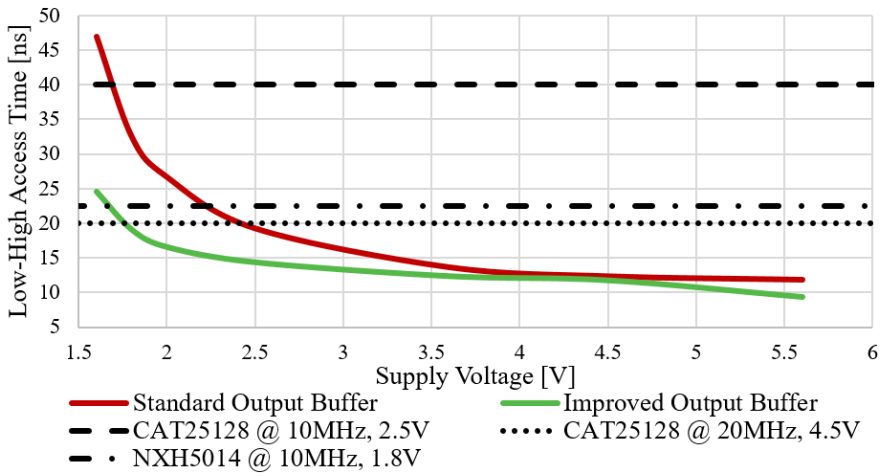

Fig. 21. SPI interface Low-High Access Time vs. Supply Voltage - comparison.

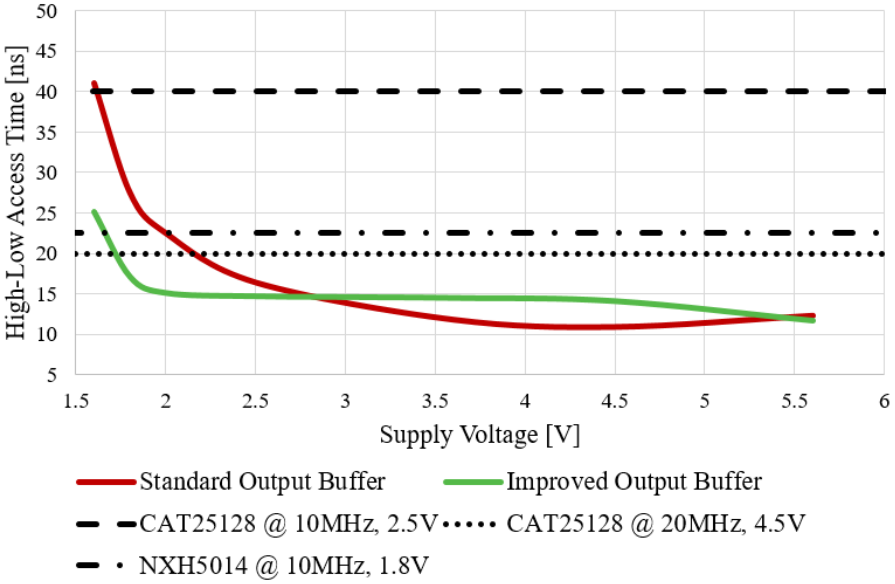

Fig. 22. SPI interface High- Low Access Time vs. Supply Voltage - comparison.

4.3. Final comparison

Table 9 shows a comparison between the performances of the standard and improved output buffer topologies, as resulting from the previously shown data. The new topology brings a significant increase in speed (the propagation time is halved), while reducing both current and area consumption. The area of the driver (*i.e.* the circuitry driving the two output transistors) in particular is reduced by nearly 80%, as a result of the extensive use of low voltage transistors

instead of high voltage ones (for the standard topology).

The new topology also reduces access times when used in serial communication interfaces: by up to ∼46% for SPI and ∼31% in I^{2}C UFm (which has 10 ns input filters, thus reducing the effect of the buffer's delay on the access time).

Table 9. Comparative performances of the two output buffer topologies

Parameter	**Standard Output Buffer**	**Improved Output Buffer**	**Improvement [%]**
t_r [ns] @1.6V	8.0	6.7	16.2
t_f [ns] @1.6V	6.7	1.2	82.0
t_p [ns] @1.6V	28.1	14.2	49.4
avg (i_{DD} [mA] @1.6V	0.34	0.29	14.7
avg (i_{DD}) [mA] @5.6V	1.28	1.03	19.5
Area Consumption without output transistors [μm^2]	2191	502	77.1
Area Consumption including output transistors [μm^2]	5647	3958	29.9
$t_{VD,DAT}$ [ns] for I^{2}C UFm	65.1	44.7	31.3
$t_{VD,DAT}$ [ns] for SPI	46.9	25.1	46.4

5. Conclusions

An improved I/O pin was designed and implemented in a 0.18μm CMOS EEPROM process with low and high voltage transistors. The circuit was tested in two types of serial mid-speed communications interfaces I^{2}C UFm and SPI.

The I/O pin is an interface between internal LV logic and a HV communication line. The input and output buffers were demonstrated, through simulations, to operate at supply voltages from 1.6V to 5.6V, with the output buffer allowing for loads of up to 3 mA.

The maximum delay of the improved output buffer is reduced by ∼50% at 1.6V – 14.2 ns compared to 28.1 ns for the standard buffer. The output rise time is reduced ∼1.3 times, while the falling edge is around 5 times faster, compared to the basic topology. These improvements allow for a higher theoretical data rate (20 Mbps instead of the initial 10 Mbps). Moreover, a reduced current consumption of the HV side (by up to 20%) was observed. Furthermore, the new topology brings a 30% reduction in area consumption with a nearly 80% reduction of the area occupied by the driver part of the buffer (*i.e.* excluding the output transistors).

The I/O pin was tested in an I^{2}C UFm interface at 5Mbps and in a SPI interface at 10Mbps, for the two limit power supply voltages, 1.6V and 5.6V. In the I^{2}C UFm interface, for the standard topology, the maximum access time at 1.6V is around 32.5% of the bit time, while for the improved one it is reduced to about 22.5%. In the SPI interface, at 10 Mbps and 1.6V, the access time with the standard buffer is ∼47% of the bit time, which makes operation unfeasible. With the new buffer, however, this is achievable, since the access time is reduced to ∼25% of the bit time.

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