Low cost approaches for High Resolution Digitally Programmable Potentiometers

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Abstract. This paper aims to find adequate solutions for implementing a high resolution digitally programmable potentiometer by taking into consideration the production cost and also the performance indicators such as the linearity characteristics, wiper resistance and total resistance variations. All described solutions were implemented in a 5V 0.18 µm CMOS process and their performances were verified by simulations.

Key-words: Digitally programmable potentiometer; high resolution; production cost; linearity characteristics; wiper resistance; total resistance variations.

1. Introduction

Digitally programmable potentiometers (DPPs) are mixed signal devices, that have the same function as a normal potentiometer, namely that of providing variable resistance, but instead of the mechanical action they use digital signals and switches.

Generally, a digitally programmable potentiometer has three terminals (high reference terminal H, low reference terminal L and wiper terminal W). It is built from a set of resistors of equal values, usually called unit, incremental or step resistors (R0) along with switches that can be selectively turned on and off by digital signals [1] in such a way to determine the resistor ratio corresponding to each step/wiper position. In order to provide this function, it needs a logic part and an analogic part (Fig. 1). Depending on the DPP type, the logic part may comprise a digital interface, registers which can store the wiper position (for non-volatile DPPs) and the decoder responsible with sending the proper command to the switches. The illustrated analog part has
the basic/conventional structure composed by resistors connected to the wiper through switches. The paper concentrates mostly on the different configurations for the analog part and takes into consideration only the decoder complexity of the digital part to show its strong dependence on the configuration chosen for the analog part.

A very important parameter of potentiometers is the resolution expressed by the number of wiper taps. Unlike the mechanical potentiometer, where the number of taps is infinite [2], because of its digital control, the digitally programmable potentiometer has the drawback of finite steps. In this case, the resolution is determined by the number of digital bits used for selecting the desired wiper position. Because higher resolution means finer adjustments and providing more output voltages in order to enlarge the area of applications for digitally programmable potentiometers the resolution should be increased. For instance, the popularity gained by digital trimming, as a solution for on-chip adjustment, resulted in an increasing demand for digital potentiometers with higher resolution, typically using more than 7 bits for controlling the wiper position [1].

But, for a basic digital potentiometer, an increase in resolution (in the number of bits) generates a steep increase in the number of required components (resistors, switches and logic circuitry for decoding). Considering an n bit resolution, where the number of steps is $2^n$, this basic implementation requires $2^n$ wiper switches and $2^n-1$ unit/step resistances [1]. So, one bit resolution increase means doubling the number of switches and resistors, and implies doubling the consumed area, which is a real concern.

To solve this issue, different methods were taken into consideration in the literature. Some of them use bulk impedance devices [1], while others use binary weighted decoding resistors [3].

Eleven most representative DPP architectures were chosen from these two categories, were adapted for an 8 bit resolution and were designed using dedicated decoders.

Firstly, the functional description of the most common or basic architecture was done in order to better understand its issues when it comes to high resolution requirements, and then the solutions to diminish these issues were described. Through the paper, this first architecture

![Fig. 1. Basic DPP structure.](image)
was considered as reference and compared from multiple points of view with the multistage architectures.

The purpose of this comparison is to study the effectiveness of the methods used in multistage architecture in reducing the required silicon area of high resolution potentiometers while maintaining good linearity characteristics [4]. There were also considered total resistance variations and wiper resistance.

All DPP architectures were designed in a 5V CMOS technology, have 256 steps (8 bit resolution), a total resistance of 10k\(\Omega\), the supply voltage \((V_{CC})\) range between 2.7V and 5.5V, and voltage limits applied on their ending terminals (L and H) between 0 and the supply \((V_{CC})\). For all architectures transfer gates switches (with both NMOS and PMOS transistors) were used.

2. Digital potentiometer architectures

2.1. Single stage (basic) architecture

Basic architecture [1, 5], often called single stage or SS (the analog part represented in Fig. 1) has the simplest configuration of a single stage (the wiper stage) composed by incremental resistors \((R_0\) of 39.2\(\Omega\)) connected to the wiper terminal by a single switch at a time. Despite its simplicity, as the number of bits of resolution increase, the number of components needed increase a lot. To be more specific, the basic configuration of a 7 bit resolution DPP requires 127 unit resistors and 128 wiper switches while an 8 bit resolution DPP requires 255 unit resistors and 256 wiper switches. This doubling in the number of components would result in a double required silicon area and consequently higher production cost. Moreover, its complexity of decoding is quite high, since each switch needs a unique command that takes into consideration all the 8 bits. For this 8 bit resolution, apart from the number of resistors and switches previously specified, 5648 transistors are also used for the decoding part.

In SS architecture, switches occupy the largest portion of the total area. So, for lowering the area and implicitly the production cost, it is desirable to use topologies that reduce the number of switches needed to provide the whole range of wiper voltages between 0 and \(V_{HL}\). Such topologies are provided by multistage architectures.

2.2. Multiple stage architecture

Generally, multistage architectures have at least two stages, one where switches commands are derived from less significant bits and the other stage where switches commands come from the combination of more significant bits. In order to keep the same value for the total resistance \((R_{HL})\) switches from upper and lower stages from both multistage categories are controlled complementarily.

Two different categories of multistage architectures were analyzed: multistage architectures using bulk resistors (in Fig. 2, schematics from B0 to B3) and multistage architectures using binary weighted resistors (in Fig. 3, schematics from BW1 to BW7).

We start by analyzing the multistage architectures that use bulk resistors. Their main purpose is to reduce the wiper stage by grouping bunches of unit resistors into bulk impedance blocks \((128' R_0, 16' R_0, 113' R_0)\). The unit resistor \((R_0)\) is 39.2\(\Omega\) for each of these four configurations.

Compared to the basic architecture, B0 architecture reduces the wiper stage to 127 unit resistors connected to the wiper terminal through one of the 128 wiper switches and groups a
bunch of 128 unit resistors into a bulk impedance block of $128^\ast R_0$. For steps below 127, SBH and SBL switches are closed and SBLH and SBHL switches are open. Under these conditions, B0 schematic works like the basic one. For steps greater than 128, the high terminal (H) is switched with the low terminal (L) through the SBLH and SBHL switches which are closed and the impedance block of $128^\ast R_0$ will contribute now to all resistor ratios. The procedure follows up the same rule of having only one wiper switch connected to the wiper. For its implementation, this schematic needs 255 unit resistors, 132 switches and 6400 decoding transistors. Although it reduces almost to the half the number of switches, this architecture has the disadvantage of introducing a lot of noise on the signal path due to the commuting of switches SBH, SBL, SBLH and SBHL.

B1 architecture diminishes B0 limitation by introducing an additional impedance block of $128^\ast R_0$ in the low side, which is shunted or not by SBL, depending on the step. Now H and L terminals do not have to interchange any more, since for steps smaller than 128, SBL switch is closed and shorts the $128^\ast R_0$ bulk impedance block from the low side, and for steps greater than 128, SBH switch is closed and shorts the $128^\ast R_0$ bulk impedance block from the high side. The command for these two switches is complementary in order to keep the same total resistance ($R_{HL}$) regardless the step. Compared with B0 architecture, for the implementation of this schematic the number of unit resistances was increased to 383, the number of switches slightly was decreased to 130 and the number of decoding transistors was reduced to half (2576).

Fig. 2. Multistage architectures using bulk resistors.
Fig. 3. Multistage architectures using binary weighted resistors.

B2 architecture reduces even more the wiper stage to only 15 unit resistors but compared to the previous schematic uses two additional shunt stages of 7 complementarily controlled groups of $2^{16}R_0$ impedance blocks. In this way the number of switches is reduced to 30, but the number of resistances increases to 495 units, while its decoding section is characterized by a lower complexity (232 transistors).

B3 architecture uses a different approach and instead of the two groups of $2^{128}R_0$, it doubles the wiper stage of 15 unit resistors and uses an additional bulk impedance of $2^{113}R_0$, while keeping the two shunt stages. For steps between 0 and 127, the connection to the wiper terminal is done through $S_{MSB,L}$ switch, which is closed, while for steps between 128 and 255, this connection is done through $S_{MSB,H}$, whose command is complementary to $S_{MSB,L}$. Within this scenario, 335 unit resistors, 48 switches and 552 decoding transistors are needed.

The analysis continues with multistage architectures that use binary weighted resistors.

The basic structure for this kind of architecture is represented in BW1 schematic, where two stages of eight resistors having binary weighted values ($2^0-2^7R_0$) and the wiper terminal connected between them are used. For this implementation 510 unit resistors of 39.2Ω, 16 switches and 16 decoding transistors are needed. It is noticeable that this approach succeeds to reduce a lot the number of switches (almost 16 times smaller compared to SS) and also the number of required decoding transistors. These statements reveal its reduced area and low decoding complexity, which are great pluses compared to the previous analyzed architectures.

BW2 architecture introduces a wiper stage of 15 resistors of $R_0/15$ responsible with the fine changes (of the less significant bits) and reduces both low and high stage to 4 resistors of binary
weighted values \((2^0 - 2^{3\times R0})\), while using a different \(R0\) value of 625Ω. High and low stages are responsible with coarse changes (of the more significant bits). This schematic contains 31 unit resistors of 625Ω, 24 switches and 144 decoding transistors but has linearity issues that will be reflected in the simulation section. These are caused by the fact that the real number of steps is not 255, but 240 because every 15 steps, two consecutive taps are equal. More precisely step 15 is equal to step 16, step 30 is equal to step 31 and so on.

BW3 architecture comes with the solution to BW2 problem, by using 15 resistors of 16\(^\ast\)R0 in the wiper stage, responsible with the coarse changes. For the low and high stages, the same BW2 structure was kept, but now these stages are responsible with the fine changes. Moreover, \(R0\) is designed to be equal to 39.2Ω. For this architecture 270 unit resistors, 24 switches, 144 decoding transistors are needed.

BW4 topology has also three stages: the wiper stage which contains fewer unit resistors (seven resistors of \(R0/7\)) and two stages (low and high) composed by 5 binary weighted resistors \((2^0 - 2^{4\times R0})\). Same as BW2, wiper stage is responsible with fine changes, while for the coarse changes high and low stages are in charge. This implementation has also the drawback of fewer than 256 steps, because every 7 steps two consecutive taps are equal. More precisely, it has only 224 real steps, since step 7 is equal to step 8, step 15 is equal to step 16, step 30 is equal to step 31 and so on. For its design 63 unit resistors of 312.5Ω, 18 switches and 64 decoding transistors are needed.

BW5 schematic comes with the solution to BW4 resolution problem and uses 7 resistors of 32\(^\ast\)R0 for the wiper stage, who is in charge now with the coarse changes. This architecture requires 286 unit resistors of 39.3Ω, 18 switches and 64 decoding transistors.

BW6 architecture is the equivalent of BW4 schematic, but now the wiper stage was replaced with two intermediate shunt stages separated by the wiper terminal. These two shunt stages work complementarily and are responsible with fine changes. The configuration used for shorting the 7 resistors of \(R0/7\) assures a constant polarization for the low side of the chain, keeping the resistance constant for all the fine changes. Of course, it has the same drawback of fewer steps, as BW4. For its design 64 unit resistors of 312.5Ω, 24 switches and 96 decoding transistors are needed.

BW7 has the same structure as BW6, but uses for the shunt stages seven resistors of 32\(^\ast\)R0 in order to solve the issue of fewer steps. In this case, shunt stages are responsible for the coarse changes of the wiper voltage. Its implementation requires 510 unit resistors of 39.2Ω, 24 switches and 96 decoding transistors.

This multistage approach using binary weighted resistors requires fewer switches and a simpler decoding circuitry compared to the bulk impedance architectures, but because of a greater number of switches needed to be closed on the H to L path, its linearity characteristics are not so good and this will be proved by the simulation section. Apart from simulations, silicon area estimations based on the number of devices and their size were done and represented in Fig. 4.

Compared to the basic architecture (SS), both multistage categories require smaller areas. The lowest values correspond to the binary weighted architectures mainly due to a decrease in the number of switches required. The reduction in area for binary weighted architectures is significant, about eight times smaller compared to single stage architecture and corresponds to BW5 configuration. For the bulk architectures the smallest area is about five times smaller than SS area and corresponds to B2 topology.

Apart from area estimation all architectures were compared also considering the linearity characteristics, total resistance variation with different parameters and wiper resistance value.
3. Performance simulations

All described architectures were designed using 5V devices, meet the total resistance value of 10kΩ and have an 8 bits resolution. For all the simulations L terminal is connected to GND and $V_H$ equals $V_{CC}$.

3.1. Linearity errors

The main problem encountered by digital potentiometers implemented using multistage architectures is that some of the resistors need to be shunted by switches. But real CMOS switches, even in ON state, exhibit a certain resistance and this generates linearity errors quantified by Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) errors, Zero-Scale Error (ZSE) and Full-Scale Error (FSE).

All these parameters will be described considering the voltage divider configuration for a potentiometer having 256 steps (k=1 to 255).

INL error is defined as the deviation between the ideal wiper voltage value (the expected one) and the actual wiper voltage value (the real one). Based on the wiper voltage measured in simulations, INL error was calculated using the following formula:

\[
INL(k) = \frac{V_{Wreal}(k) - V_{Wideal}(k)}{V_{LSB}}
\]  

On the other side, DNL error refers to the deviation of the step variation from one tap to another [3], and for its calculation the following formula was used:
\[ DNL = \frac{V_{W_{\text{real}}(k)} - V_{W_{\text{real}}(k-1)} - V_{\text{LSB}}}{V_{\text{LSB}}} \] (2)

ZSE error is defined as the difference between an ideal and actual potentiometer output when zero digital code is applied to the input. Based on the simulation results for the wiper voltage, ZSE was calculated using the formula:

\[ ZSE = \frac{V_{W_{\text{real}}(0)}}{V_{\text{LSB}}} \] (3)

FSE is defined as the difference between an ideal and actual potentiometer output when full scale digital code is applied to the input and for its calculation the following formula was used:

\[ FSE = \frac{V_{W_{\text{real}}(225)} - V_{HL}}{V_{\text{LSB}}} \] (4)

All linearity errors are measured in LSB (Least Significant Bit) values. In digitally controlled potentiometers case, one LSB is equivalent to the voltage difference between H and L, divided by the total number of steps, and its formula is written below:

\[ V_{\text{LSB}} = \frac{V_{HL}}{255} \] (5)

Usually, for a digital potentiometer with 256 steps INL limit is ±1LSB, DNL limit is ±0.5LSB and ZSE and FSE limits are ±0.5LSB [6].

All the described architectures were subject to INL, DNL, ZSE and FSE simulations and the results are presented in the next paragraphs.

Each error was analyzed for two different supply voltages \( V_{CC} = 2.7V \) and \( V_{CC} = 5.5V \) in order to see the influence of switches for both low and high voltages.

Figs. 5-6 illustrate the INL error for \( V_{CC} = 2.7V \), while Figs. 7-8 illustrate INL error for \( V_{CC} = 5.5V \).

For \( V_{CC} = 2.7V \) INL values stay under 0.85LSB for those using bulk resistors and exceed the datasheet limit of 1LSB almost for all binary weighted architectures, excepting BW6.

For \( V_{CC} = 5.5V \) INL values are smaller for both multistage categories, but great differences still exist between them (approximately one order of magnitude). In both cases it can be observed that SS and B0 architectures are the most linear and the explanation is that there are no resistances shorted by switches from H to L path, while architectures using binary weighted resistors introduce the greatest linearity errors. These errors are higher for \( V_{CC} = 2.7V \) because of the nature of CMOS switches whose \( R_{ON} \) increases with the decrease of the supply voltage.
Fig. 5. INL error for single stage architecture and multistage architectures using bulk resistors when $V_{CC}=2.7V$.

Fig. 6. INL error for multistage architectures using binary weighted architectures when $V_{CC}=2.7V$.

DNL errors were also calculated for all architectures considering the same two values for the supply voltage $V_{CC}=2.7V$ (Figs. 9-10) and $V_{CC}=5.5V$ (Figs. 11-12).

SS and B0 have the smallest DNL error in both cases, while all other bulk architectures respect DNL datasheet limit of 0.5LSB for $V_{CC}=5.5V$, but only B1 and B3 respect it also for $V_{CC}=2.7V$. As it concerns the multistage architectures using binary weighted resistors, none of them comply with the DNL datasheet limit.

Apart from INL and DNL errors, just like a digital to analog converter, a digital potentiometer is characterized by zero scale and full scale errors (ZSE and FSE). Essentially, these parameters describe the residual resistance that may occur at the top and bottom of the potentiometer [7].
They are also important parameters because they allow the user to know if the potentiometer enables adjustments that meet zero level (GND) and full scale level ($V_{H.L.}$). For instance, in audio applications, zero level close to GND is desired in order to provide better isolation.

The values for ZSE and FSE were calculated using formulas (3) and (4) and they were recorded in Table 1.

![Fig. 7. INL error for single stage architecture and multistage architectures using bulk resistors when $V_{CC}$=5.5V.](image1)

![Fig. 8. INL error for multistage architectures using binary weighted architectures when $V_{CC}$=5.5V.](image2)
Fig. 9. DNL error for single stage architecture and multistage architectures using bulk resistors when $V_{CC}=2.7V$.

Fig. 10. DNL error for multistage architectures using binary weighted architectures when $V_{CC}=2.7V$.

As expected, the values obtained for both ZSE and FSE for $V_{CC}=2.7V$ are greater than the values obtained for $V_{CC}=5.5V$ and this is due to the higher values for switches $R_{ON}$ at lower supply voltages. The values obtained for ZSE are in strong correlation with the number of closed switches when zero code is applied. The best values were those corresponding to SS and B0 architecture. The maximum number of closed switches is eight and corresponds to BW1 archi-
tecture whose ZSE has the maximum value. As it concerns FSE, SS and B0 introduce the smallest errors, while the greatest value is obtained for BW6 due to its configuration for which the maximum wiper voltage value for the last step equals theoretically \( \frac{31}{32} V_{HL} \) and not \( \frac{32}{32} V_{HL} \).

Fig. 11. DNL error for single stage architecture and multistage architectures using bulk resistors when \( V_{CC}=5.5V \).

Fig. 12. DNL error for multistage architectures using binary weighted architectures when \( V_{CC}=5.5V \).
The worst linearity values were obtained for BW2 and BW4. This is a consequence of the fact that their design has an issue and the real number of steps is not 256, but 240 or 224, because every 15 or 7 steps, two consecutive taps are equal. Although, BW6 has the same issue, it seems that this new configuration implying shunt stages to be responsible with the fine changes helps in the reduction of errors. Moreover, this configuration becomes less dependent on the applied voltages (small differences between errors when $V_{CC}=2.7\,\text{V}$ and $V_{CC}=5.5\,\text{V}$). Compared with BW7, which has the same structure but different values for ladder resistances in order to diminish the issue of smaller resolution, BW6 is still the one who exhibits smaller errors. One explanation for this can be the fact that the influence of $R_{ON}$ switches shorting the binary weighted resistors is higher when shorting smaller resistances values (24*R0=627.2Ω for BW7 compared to 24*R0=5000Ω for BW6).

Because multistage architecture using binary weighted resistors introduce great errors, they are not recommended to be used in high accuracy application. They should rather be used in applications where the occupied area is more important than linearity.

Apart from switches which have a great influence on the accuracy of a digital potentiometer, in reality there are also other factors such as: device matching, parasitic devices, the spread of technological parameters, the variations with the operating conditions that affect it [1]. So, in order to be sure that in reality a DPP respects the datasheet linearity limits, there should be considered the configuration that assures the smallest linearity errors in simulations. In our case, B1 and B3 are the most recommended architectures to be used in applications that require high precision.

### Table 1. ZSE and FSE errors for all architectures

<table>
<thead>
<tr>
<th>DPP type</th>
<th>ZSE@$V_{CC}=2.7,\text{V}$ [LSB]</th>
<th>FSE@$V_{CC}=2.7,\text{V}$ [LSB]</th>
<th>ZSE@$V_{CC}=5.5,\text{V}$ [LSB]</th>
<th>FSE@$V_{CC}=5.5,\text{V}$ [LSB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SS</td>
<td>0.00003</td>
<td>2.0004</td>
<td>0.0001</td>
<td>0</td>
</tr>
<tr>
<td>B0</td>
<td>0.3599</td>
<td>2.2342</td>
<td>0.1984</td>
<td>2.1307</td>
</tr>
<tr>
<td>B1</td>
<td>0.3592</td>
<td>2.2374</td>
<td>0.1466</td>
<td>0.1214</td>
</tr>
<tr>
<td>B2</td>
<td>0.7115</td>
<td>2.4713</td>
<td>0.2918</td>
<td>0.2419</td>
</tr>
<tr>
<td>B3</td>
<td>0.3524</td>
<td>2.2344</td>
<td>0.1454</td>
<td>0.1206</td>
</tr>
<tr>
<td>BW1</td>
<td>2.6665</td>
<td>3.6030</td>
<td>1.1315</td>
<td>0.9434</td>
</tr>
<tr>
<td>BW2</td>
<td>1.3952</td>
<td>3.0482</td>
<td>0.5836</td>
<td>0.4839</td>
</tr>
<tr>
<td>BW3</td>
<td>1.7335</td>
<td>3.4246</td>
<td>0.5496</td>
<td>0.4602</td>
</tr>
<tr>
<td>BW4</td>
<td>1.2440</td>
<td>2.6492</td>
<td>0.9602</td>
<td>2.9190</td>
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<tr>
<td>BW5</td>
<td>1.5957</td>
<td>2.8852</td>
<td>0.9221</td>
<td>2.5074</td>
</tr>
<tr>
<td>BW6</td>
<td>2.0150</td>
<td>3.6188</td>
<td>1.1284</td>
<td>3.0345</td>
</tr>
<tr>
<td>BW7</td>
<td>1.9513</td>
<td>3.1235</td>
<td>1.1183</td>
<td>2.6400</td>
</tr>
</tbody>
</table>

### 3.2. Total resistance variations

Another interesting simulation is the variation of the total resistance ($R_{HL}$) with the step number illustrated in Figs. 13-14. Unlike the single stage architecture, where total resistance remains constant regardless the step, in multistage architectures $R_{HL}$ varies from step to step. It
can be observed that the curves change their shapes at different steps and this is due to the fact that the influence of switches is changing with the step number. As the step changes, the voltage applied on the switches changes and in this way they contribute with a different ON resistance value. Taking B1 architecture as example, for steps below 128, the resistance value introduced by SBL switch is greater than the resistance value introduced by SBH switch for steps greater than 128 and this can be seen from B1 total resistance variation curve which is higher for steps below 128 and lower for steps over 128.

From these plots, tolerance error defined as the difference expressed in percent between the value obtained in simulations for $R_{HL}$ and the nominal value of 10kΩ can be extracted. The maximum simulated tolerance error is about 1.2% and corresponds to BW1 and BW6. Usually, datasheet potentiometer resistance tolerance is 20% [6].

Because the resistive nature of these analog switches is more susceptible to process variations, voltage, and temperature than the unit resistors (R0) in the resistor ladder [8], their influence in the total resistance is greater than the one obtained by simulation. This kind of mismatches, together with unit resistance mismatches can generate great loses in resolution, mostly in applications that do not allow calibration routine to adjust the wiper position of the digital potentiometer and adjust for any offset [9], but this kind of variations were not considered in the simulations.

![Fig. 13. $R_{HL}$ variation with step number when $V_{CC}=2.7V$.](image-url)
In order to see the influence of temperature in DPP total resistance, the TCR (temperature coefficient of resistance) is calculated using formula:

$$\text{TCR} = \frac{\Delta R_{HL}}{\Delta T} \frac{1}{R_{HL}}$$  \hspace{1cm} (6)

$R_{HL}$ variation with temperature was simulated considering the potentiometer set at the middle scale and the results were presented in Fig.15. It seems that the most affected schematics are BW4, BW6 and BW2 which exceed the datasheet limit of 100ppm/°C [6].

DPP temperature coefficient of resistance is affected by $R_0$ variation with temperature, but also by switches $R_{ON}$ resistance variation with temperature. Unit resistors of 39.2Ω (used in SS, B0-B4, BW1, BW3, BW5 and BW7 architectures) have a TCR of −99ppm/°C, while unit resistors of 625Ω (used in BW2 architecture) and 312.5Ω (used in BW4 and BW6 architectures) have a TCR of −162ppm/°C. These TCR values have different values for different $R_0$ values because they were designed with different width and lengths. Though, the potentiometer TCR values obtained for the described architectures are smaller than these unit resistors TCR values. The explanation is that the switches from H to L path contribute with a positive TCR and in this way they partially compensate for the TCR of incremental resistors.

Fig. 14. $R_{HL}$ variation with step number when $V_{CC}=5.5\text{V}$. 

In order to see the influence of temperature in DPP total resistance, the TCR (temperature coefficient of resistance) is calculated using formula:
3.3. Wiper resistance

For applications where significant currents are drawn through the wiper, wiper resistance should be taken into account. This is a very important parameter for digitally programmable potentiometers and it is defined as the resistance added by the wiper connection. In the majority of cases, this wiper resistance is equivalent with the ON resistance of the switch connecting the resistor ladder to the wiper terminal. Simulations were done for determining the wiper resistance for all architectures and the results were illustrated in Figs. 16-17. These simulations were done for $V_{CC}=3.3\text{V}$ and $I_{load}=0.3\text{mA}$ current flowing through the wiper terminal, while H terminal was left floating.

$$R_{\text{wiper}} = \frac{V_{W} - V_{H}}{I_{load}}$$  \hspace{1cm} (7)

It can be observed that BW1, BW6 and BW7 exhibit almost zero wiper resistance and this is due to the fact that they do not have a wiper stage to interconnect the resistor ladder to the wiper terminal but connect it directly. All the other architectures, excepting B3, have a maximum 17Ω wiper resistance. B3 has two switches connected to the wiper at a time (one of SWL0-SWL15 and S_MSB_L or one of SWH0-SWH15 and S_MSB_H), so the value for its wiper resistance is double.

So, for applications where high wiper currents exist, the most indicated topologies are the ones with the smallest value for the wiper resistance, namely BW1, BW6 and BW7.
Fig. 16. Wiper resistance for single stage architecture and multistage architectures using bulk resistors.

Fig. 17. Wiper resistance for multistage architectures using binary weighted resistors.
Table 2 summarizes the results of our analysis, focusing on the silicon required area, INL and DNL linearity errors (the maximum simulated values for them considering the two different values for $V_{CC}$), wiper resistance and TCR. Those parameters that exceed datasheet limits are bolded.

Table 2. Performance parameters comparison

<table>
<thead>
<tr>
<th>DPP type</th>
<th>Silicon Area [$\mu$m$^2$]</th>
<th>INL max [mLSB] @2.7V</th>
<th>INL max [mLSB] @5.5V</th>
<th>DNL max [mLSB] @2.7V</th>
<th>DNL max [mLSB] @5.5V</th>
<th>Wiper resistance [Ω]</th>
<th>TCR max [ppm/°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SS</td>
<td>204,720</td>
<td>5.7</td>
<td>4.2</td>
<td>0.32</td>
<td>0.1</td>
<td>17</td>
<td>-99</td>
</tr>
<tr>
<td>B0</td>
<td>112,291</td>
<td>6.3</td>
<td>5.8</td>
<td>1.63</td>
<td>0.9</td>
<td>17</td>
<td>-97</td>
</tr>
<tr>
<td>B1</td>
<td>111,022</td>
<td>360</td>
<td>74</td>
<td>296</td>
<td>165</td>
<td>17</td>
<td>-98</td>
</tr>
<tr>
<td>B2</td>
<td>36,914</td>
<td>830</td>
<td>44</td>
<td>1470</td>
<td>112</td>
<td>17</td>
<td>-96</td>
</tr>
<tr>
<td>B3</td>
<td>46,181</td>
<td>200</td>
<td>84</td>
<td>290</td>
<td>164</td>
<td>34</td>
<td>-98</td>
</tr>
<tr>
<td>BW1</td>
<td>26,600</td>
<td>1100</td>
<td>530</td>
<td>1244</td>
<td>880</td>
<td>0</td>
<td>-89</td>
</tr>
<tr>
<td>BW2</td>
<td>24,553</td>
<td>1020</td>
<td>970</td>
<td>1620</td>
<td>1160</td>
<td>17</td>
<td>-156</td>
</tr>
<tr>
<td>BW3</td>
<td>25,870</td>
<td>1025</td>
<td>520</td>
<td>1230</td>
<td>700</td>
<td>17</td>
<td>-95</td>
</tr>
<tr>
<td>BW4</td>
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<td>1020</td>
<td>998</td>
<td>1650</td>
<td>1170</td>
<td>17</td>
<td>-155</td>
</tr>
<tr>
<td>BW5</td>
<td>21,773</td>
<td>1410</td>
<td>815</td>
<td>1550</td>
<td>900</td>
<td>17</td>
<td>-94</td>
</tr>
<tr>
<td>BW6</td>
<td>44,366</td>
<td>920</td>
<td>885</td>
<td>970</td>
<td>990</td>
<td>0</td>
<td>-154</td>
</tr>
<tr>
<td>BW7</td>
<td>32,720</td>
<td>1310</td>
<td>776</td>
<td>1440</td>
<td>850</td>
<td>0</td>
<td>-91</td>
</tr>
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</table>

For applications where the production cost is very important, multistage architectures using binary weighted resistors should be used. They also came with the advantage of lower decoding complexity. Some of them (BW1, BW6 and BW7), are the best choice when talking about applications where significant current flows through the wiper terminal because of their zero wiper resistance. Though, for applications working at high supply voltages (5.5V) while potentiometer should have small area, good linearity and acceptable $R_{HL}$ variations, BW1 and BW3 topologies are the most recommended. In high precision applications, the most linear architecture that should be used is the basic one (SS), but the price paid for this is the huge area it requires.

Though, good linearity and acceptable silicon area (to eight times smaller than the SS area) are offered by architectures using bulk resistors. No matter what supply voltage is used, the smallest errors correspond to B0 configuration, which succeeds in the reduction to the half of the area compared to SS. Unfortunately, B0 has a great limitation due to the noise introduced by the switching of terminal H with terminal L through direct switches connected on the signal path.

For high voltage applications that need good linearity, B2 topology is the most proper to be used since it respects INL, DNL, ZSE, FSE and TCR datasheet limits, while occupying the smallest area from all multistage categories using bulk resistors (five times smaller compared to SS area).

Overall, B3 schematic can be considered a good compromise since it respects the DNL, INL, ZSE and TCR datasheet limits for both low and high voltages while occupying a reasonable area.
4. Conclusions

Twelve high resolution (8 bits) DPP architectures were compared through multiple simulations taking into consideration the required silicon area, linearity characteristics (INL, DNL, ZSE, FSE), total resistance variations with step and temperature, and wiper resistance. SS architecture was considered as reference when compared to multistage architectures coming from two different categories: multistage architectures using bulk resistors and multistage architectures using binary weighted resistors.

There is not a final hierarchy between the analyzed architectures. It all depends on which DPP parameter is more critical for a specific application. For instance, multistage architectures using binary weighted resistors offer the most cost effective solution together with a very low decoding complexity. A significant number of topologies from this category offer the best solution when comes to wiper resistance. Though, they are not recommended in high precision application where architectures using bulk resistors are the best choice if silicon required area is a concern.

References