ROMANIAN JOURNAL OF INFORMATION SCIENCE AND TECHNOLOGY
Volume 28, Number 2, 2025, 150–160
doi: 10.59277/ROMJIST.2025.2.03

Circuit Techniques for Enhancing Output Current Accuracy in Floating Gate Drivers

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Abstract. This paper introduces two innovative circuit techniques developed to dynamically compensate output current variations in high-voltage floating gate drivers. They can be efficiently used during both charge and discharge phases, significantly reducing the sensitivity of the output current to supply voltage fluctuations. A summary of prior art is presented, reviewing a conventional gate driver architecture and its associated challenges, particularly the limitations arising from supply voltage variations that cause output current inaccuracies. These shortcomings are highlighted as key motivations for the proposed advancements. In addition to introducing the compensated architectures, the paper provides a comparative analysis of the conventional and improved designs. This analysis highlights enhancements in driving accuracy while maintaining area efficiency. One of the proposed techniques has been successfully implemented in the design of a gate driver for motor control using a standard high-voltage 0.18µm BCD technology. The proposed solutions improve performance significantly, reducing output current deviation from 25% in uncompensated designs to below 2% across the full output range (1mA – 150mA). Experimental results confirm the accuracy of the simulations, validating the effectiveness of the proposed approach.

Key-words: Automotive; BCD technology; channel length modulation; current compensation; dynamic performance optimization; high-voltage floating gate drivers; motor control.

1. Introduction: Gate Drivers in Motor Control Applications

In motor control applications, gate drivers play a crucial role in controlling the switching behavior of power devices, such as power MOSFETs or IGBTs, which are responsible for driving

the motor [1–7]. These switching devices can be either integrated on-chip or exist as external discrete components. This paper focuses specifically on gate drivers that operate with external power switches and introduces two innovative circuit techniques aimed at enhancing output current precision [8].

A typical motor control circuit includes an external half-bridge configuration (Fig. 1), which consists of a high-side (HS) switch and a low-side (LS) switch. These switches are controlled by integrated gate drivers, which ensure efficient and precise operation of the power transistors. The high-side gate driver and low-side gate driver work together to regulate current flow through the motor, controlling its torque and speed [1–7].

A gate driver's primary function is to charge and discharge the power switch's gate capacitance by supplying or sinking a controlled current, enabling transitions between ON and OFF states at specific voltage levels. Because discrete power switches differ in type, size, and total gate charge, the gate driver must accommodate a wide range of gate capacitances. To accommodate this variability, modern gate drivers typically provide over 32 configurable charge and discharge current settings, ranging from below 1mA to hundreds of milliamperes. [1, 3].

One of the most critical parameters of a gate driver is its output current precision, as this directly influences key performance factors, including switching speed, rise and fall times, and overall power losses. Higher precision enables optimized efficiency, reduced electromagnetic interference (EMI), and better thermal management, making it essential for high-performance motor control applications in automotive, industrial, and power electronics [9–12].

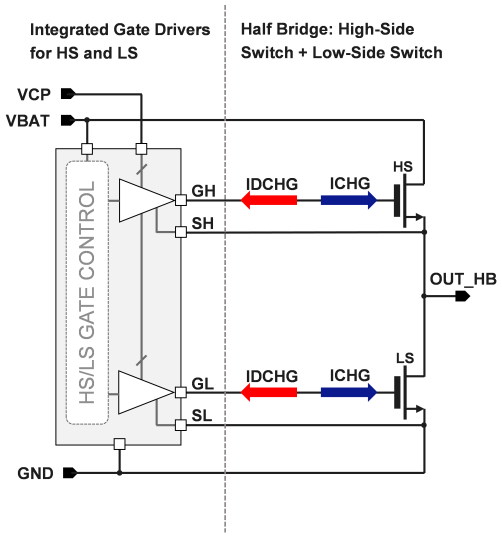

Fig. 1. Half Bridge Configuration.

In full-bridge motor control architectures (Figure 2), such as those used in brushless DC (BLDC) motors, three half-bridges are used to drive the three motor phases [1–8]. The output voltage of a half-bridge alternates between ground (0V) and the battery supply voltage (typically 12V in automotive applications). Since the high-side control circuitry is referenced to the switching node (SHx pin), which dynamically oscillates between these two levels, this configuration is called a floating gate driver. The primary challenge in driving the high-side switch is ensuring that its gate voltage is sufficiently elevated relative to its source potential for full conduction.

To achieve this, the high-side gate must be driven approximately 10V above the battery voltage, meaning a total drive voltage of 22V is required for a 12V system. This is typically provided by a charge pump circuit, generating an auxiliary rail (VCP) to supply the floating gate driver [8].

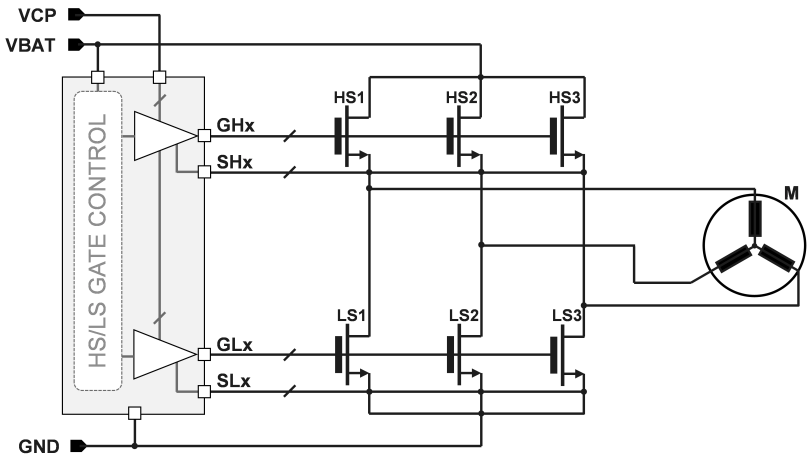

Fig. 2. Typical motor control application.

During the charging phase, the voltage difference between the VCP supply and the high-side gate starts at its maximum potential and progressively decreases as the gate capacitance charges. This dynamic voltage variation affects the precision of the gate driver's charge current due to its inherent output impedance, introducing potential deviations in switching performance. Moreover, uncontrolled slew rates during high-side transitions can result in excessive EMI emissions, posing challenges in automotive and industrial compliance [9–13]. To address these limitations, modern gate driver architectures integrate advanced compensation techniques, as the ones presented in Section 4.

2. Typical Gate Driver Architecture: Problem description

A typical control circuitry for an active power stage (High Side Gate Driver - HSx or Low Side Gate Driver - LSx) is illustrated in Fig. 3. It consists of two main blocks: the **Driving Stage** that contains the charge and discharge devices and a **VGS Reference** [8, 11]. For the sake of simplicity and clarity, the below explanations will be given in regards only to the high side.

The **VGS Reference** contains the reference transistor, M_{ref}, which is biased with a controlled reference current, I_{ref}. M_{ref} operates in saturation and will have a corresponding V_{GS} voltage equal to:

$$V_{GS} = V_T + \sqrt{\frac{2I_{\text{ref}}L}{\mu CW}} \tag{1}$$

where:

- V_T is the threshold voltage,
- I_{ref} is the reference current,

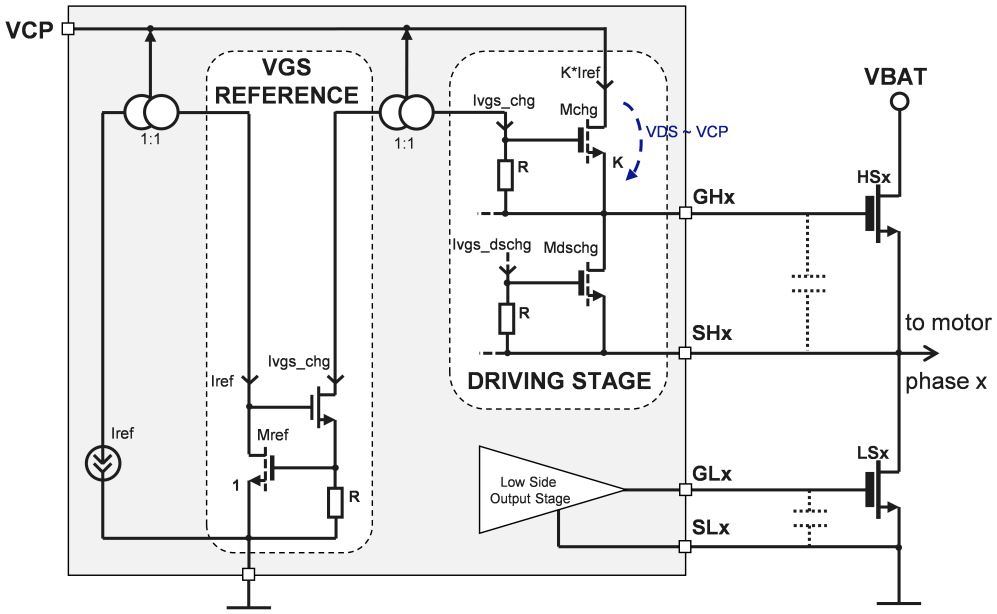

Fig. 3. Typical control circuitry of an active high-side device.

- μ is the mobility,
- C is the specific gate capacitance,
- W and L are the channel width and length, respectively.

The V_{GS} voltage is afterwards converted into an I_{vgs} current through a resistor, R. The relationship between the reference current and the I_{vgs} current is given by:

$$I_{vgs} = \frac{V_T + \sqrt{\frac{2I_{\text{ref}}L}{\mu CW}}}{R} \tag{2}$$

The I_{vgs} is transported to the output stages and applied across an identical resistor, in the gate of the charge transistor, or in the gate of the discharge transistor, ensuring that the output stage devices have the same V_{GS} as the reference transistor [8, 11]. If the output stage devices are matched with the reference devices—having the same type, finger geometry, and orientation—the charge and discharge currents will be K times higher than the reference current, where K is the area ratio between the output devices and the reference device [8, 11]:

$$I_{\text{chg, ideal}} = K \cdot I_{\text{ref}} \tag{3}$$

The only source of mismatch between these transistors is given by the major difference in their V_{DS} values. The reference transistor has a V_{DS} equal to two V_{GS} (see **Fig. 3**), while the output stage devices can have a V_{DS} equal to the CP voltage at the start of the charge phase [8, 11]. Consequently, the charge current is prone to significant deviations due to the channel length

modulation effect.This ultimately translates in a charging current error caused by the finite output resistance of the charge transistor:

$$I_{\text{chg\_real}} = K I_{\text{ref}} (1 + \lambda V_{\text{CP}}) \tag{4}$$

where λ stands for the channel length modulation effect parameter. The error in the charging current can thus be described as:

$$I_{\text{chg, err}} = K I_{\text{ref}} \lambda V_{\text{CP}} = \alpha I_{\text{ref}} \tag{5}$$

Fig. 4 illustrates the relationship between the charge current (I_{chg}) and the charge pump supply voltage, V_{CP}, under the maximum current setting, which is specified at 150mA. The graph demonstrates the behavior of the charge current across the full range of V_{CP} values, highlighting a critical performance limitation.

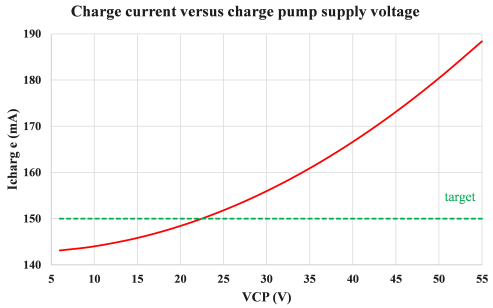

Fig. 4. Output charge current variation with the charge pump voltage without any compensation.

From the default V_{CP} value (of around 25V) to the maximum V_{CP} value, the observed variation in charge current is approximately 20%. This deviation is considerably higher than the acceptable threshold for high-performance gate drivers, which are expected to deliver high currents with a precision of 15% or better. Such a large variation compromises the reliability and consistency of the driver's performance, particularly in applications requiring stringent current accuracy.

This analysis underscores the need for improved design or calibration of the gate driver to ensure compliance with the required accuracy specifications. Enhancing the stability of the charge current over the operating range of V_{CP} is crucial for meeting industry standards and achieving optimal performance in critical applications. The following section discusses existing solutions that have been proposed to address these challenge.

3. Prior Art

Previous attempts to address the fluctuations in the output charge current versus V_{CP} (ultimately, V_{DS} of the charge transistor) have explored two main approaches. The first approach involved increasing the channel length of the transistor. In order to deliver the same current, the width-to-length (W/L) ratio has to remain constant. Hence, increasing the channel length results in a quadratic increase in the transistor area. In designs with multiple driving stages—such as those with six driving stages (3 HS and 3 LS) and six charge transistors—this quadratic area increase leads to a substantial chip area expansion, rendering the solution non-profitable [8, 9].

The second approach (Fig. 5) involves the use of a cascode configuration for the charge transistor [11]. In this method, the gate of the cascode transistor is biased by a floating supply (referred to as SHx), which helps limit the V_{DS} of the charge transistor to a reasonable range. However, the implementation of a cascode requires an additional high-voltage (HV) transistor capable of withstanding currents in the range of hundreds of milliamperes, causing area increase.

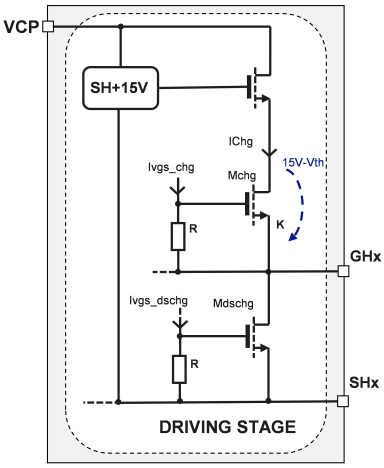

Fig. 5. Driving stage with cascoded charge transistor.

Ultimately, both approaches result in a substantial increase in chip area, highlighting the need for a circuit technique that achieves the required precision while minimizing the impact on chip area. The following section introduces two novel compensation techniques designed to enhance output current precision while maintaining efficiency and minimizing area overhead.

4. Proposed Solutions

This section presents two novel architectures designed to improve output current precision. One method achieves this by adjusting the reference current, I_{ref}, while the other compensates for variations by modifying the I_{vgs} current. These approaches are referred to as the I_{ref} compensation and I_{vgs} compensation techniques, respectively [8, 14].

4.1. I_{ref} compensation

The first proposed method, referred to as I_{ref} compensation (Fig. 6), focuses on compensating the reference current and is applied exclusively in the VGS reference stage.

This method introduces an additional branch containing a sense transistor (M_{sns}) that shares the same V_{GS} as the reference transistor (M_{ref}). However, its V_{DS} is set to the V_{CP} level minus one V_{GS}. As a result, the drain current of the sense transistor is influenced by channel length modulation in the same way as the output stage transistor, causing it to be slightly higher than the reference current. The difference between these two currents constitutes the error current (αI_{ref}), which is subsequently replicated using a current mirror (M_1-M_2) . This error current is subtracted from the drain current of the reference transistor, effectively biasing M_{ref} at a reduced

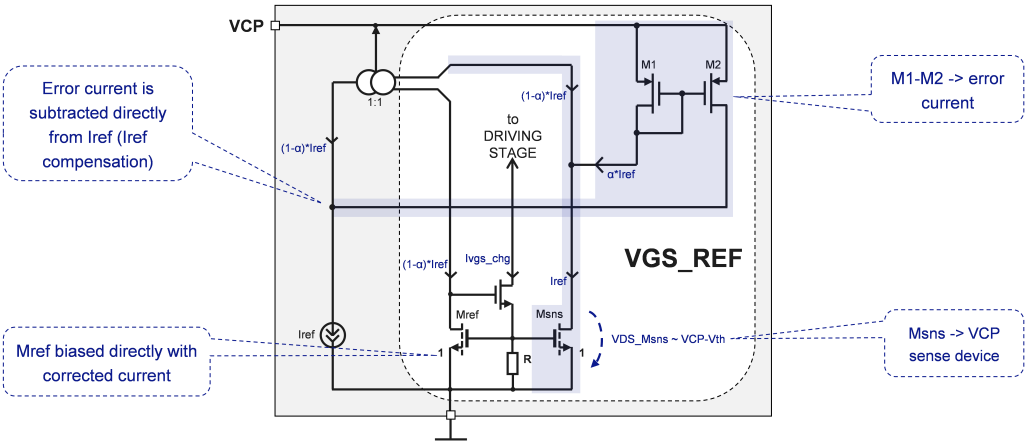

Fig. 6. I_{ref} compensation architecture.

current, (1-α)I_{ref}, to compensate for the channel length modulation effect in the output stage transistor. This current correction loop features a single inversion, ensuring inherent stability under all operating conditions.

Compared to the classical circuit configuration described in Section 2, only a limited number of additional devices have been introduced: the sense transistor (M_{sns}), which is compact in size and equal to the reference transistor (scaled by a factor of K relative to the output stage transistor), and a current mirror (M_1-M_2) that handles low currents.

4.2. I_{vgs} compensation

The second proposed method, referred to as I_{vgs} compensation, is exclusively applied to the driving stage (Fig. 7). Similar to the first method, a sense transistor($M_{\text{chg\_sns}}$) is employed within the driving stage.

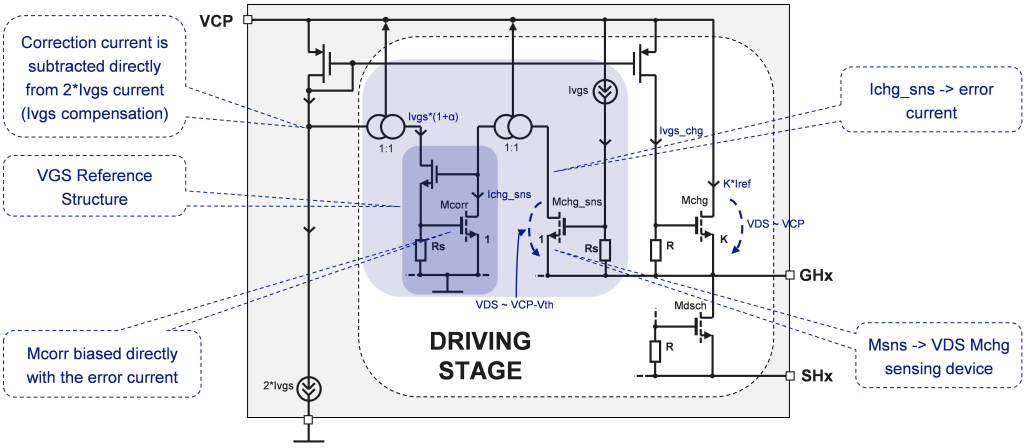

Fig. 7. I_{vgs} compensation architecture.

This sense transistor operates with the same V_{GS} and V_{DS} as the charge transistor, ensuring that its drain current is influenced by the channel length modulation effect. The drain current of the sense transistor is then converted into an $I_{\text{vgs\_corr}}$ current through the VGS Reference structure. This current is slightly higher than the I_{vgs} that is transported to the Driving stage, containing a factor which reflects the channel length modulation effect:

$$I_{vgs\_corr} = I_{vgs}(1 + \alpha) \tag{6}$$

By subtracting this $I_{\text{vgs\_corr}}$, which incorporates the correction factor, from $2I_{\text{vgs}}$, a slightly reduced $I_{\text{vgs\_chg}}$ is obtained for the charge transistor.

$$I_{vgs\_chg} = I_{vgs}(1 - \alpha) \tag{7}$$

This adjustment effectively compensates for the undesired phenomenon caused by channel length modulation by biasing the output stage transistor with a lower $V_{\text{GS}} = I_{\text{vgs\_chg}}\text{R}$. As with the I_{ref} compensation method, the current correction loop in this approach features a single inversion, ensuring stability under all operating conditions.

The primary drawback of the first method is its higher static current consumption due to the additional branch in the VGS Reference required to bias M_{sns}. In contrast, the second method does not introduce any static power consumption. However, the I_{ref} compensation method delivers superior performance when the ratio between the minimum and maximum current settings of the driver is significantly large (greater than 50).

5. Results

A plot illustrating the charge current error as a function of the charge pump voltage for both the minimum output current of 1 mA and the maximum output current of 150mA is presented in Fig. 8. The red curve represents the simulation results in the absence of any compensation, while the black curves correspond to the I_{ref} and I_{vgs} compensation techniques, respectively.

Simulation results indicate that, for both extreme values of the charge current, the deviation can reach up to 25% when no compensation is applied. However, with the implementation of a compensation technique, the deviation is reduced to below 2% in all cases. The I_{ref} compensation method has been successfully implemented into one of Infineon's latest gate driver designs. Bench measurements (green curve) confirm this approach's effectiveness, with errors staying below 2%, proving the method's robustness and practical applicability.

Fig. 9 presents a comparative analysis of the transient response of the charge current under the same three scenarios. The red curves, representing the uncompensated case, deviate significantly from the target values of 1mA and 150mA, respectively. In contrast, the black curves, corresponding to the compensated circuits, consistently maintain the target values throughout the entire charging phase of the high-side (HS) switch. The architecture implementing the I_{ref} compensation method has undergone further optimization to enhance response time, which accounts for the shorter response time observed in the figure. However, response time is beyond the scope of this study, as the primary focus is on accuracy. The results demonstrate that both compensation methods significantly improve charge current accuracy, effectively addressing the identified issue.

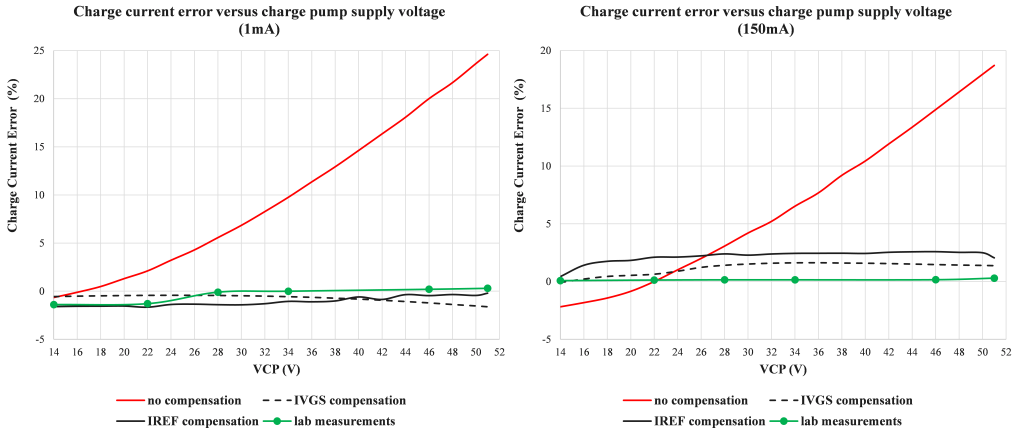

Fig. 8. Gate driver's output current error for the minimum current setting - left and the maximum current setting - right.

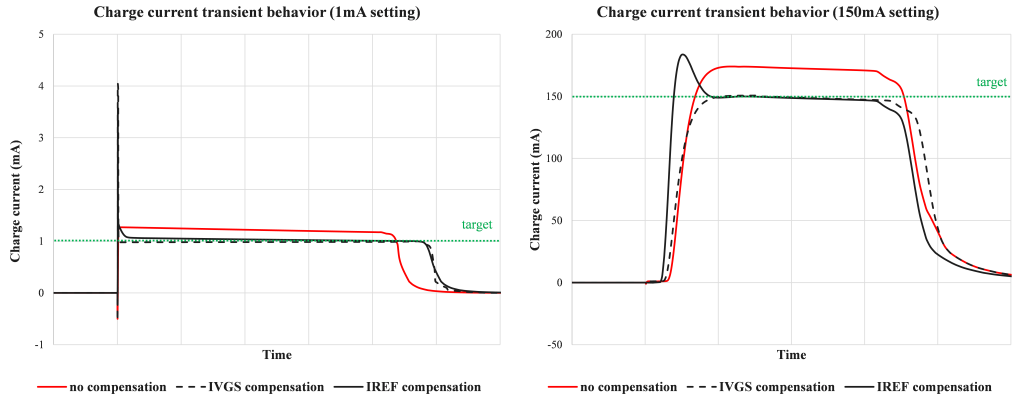

Fig. 9. Transient behavior of the driver's current for 1mA setting - left, 150mA setting - right.

To evaluate the robustness and consistency of the proposed circuit, a statistical analysis was conducted on a lot of 300 fabricated units. The results are presented in Fig. 10. The parameter under investigation is the output charge current for the minimum and the maximum current setting. Measurements were performed at room temperature, for the maximum value of the charge pump voltage, of 51V, under identical test conditions to ensure reliability and repeatability.

For the minimum current, the results exhibit a Gaussian distribution, with a mean value of around 1mA and a standard deviation of 0.052 mA, confirming the expected statistical behavior. The spread of the values remains within 35% of the nominal specification, ensuring a cpk of around 2.0. Also, for the maximum current setting, a mean value of around 150mA is obtained and a sigma of 4.2 mA, yielding a spread of around +/-17% for a cpk of 2.0. Without the proposed compensation techniques, these results would not have been possible, as channel length modulation alone introduces a systematic error of approximately 25% at the maximum charge pump value.

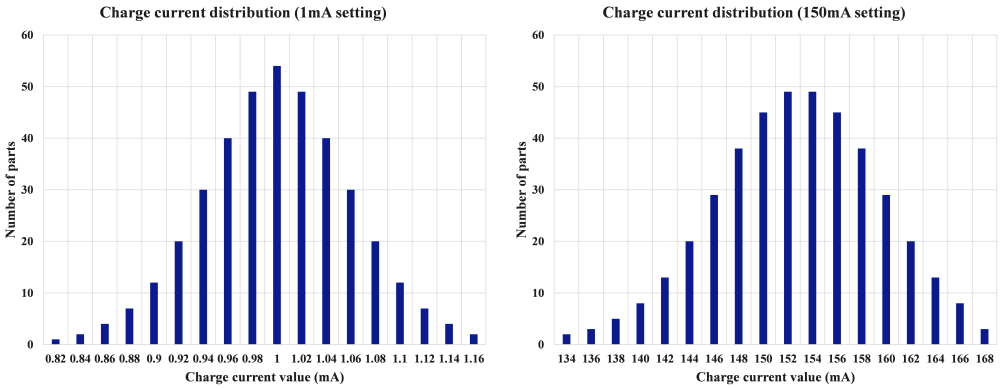

Fig. 10. Experimental distribution of the charge current for 1mA setting - left, 150mA setting - right.

These results demonstrate the effectiveness of the proposed compensation techniques, which have already been successfully implemented in a recently developed product. Their ability to significantly improve the precision of gate drivers while maintaining practical feasibility highlights their potential for widespread adoption in future high-performance applications.

6. Conclusions

In conclusion, this work addresses the significant impact of the voltage drop across the output stage on the output current of gate drivers. It presents a typical gate driver control circuitry, highlighting its inherent disadvantages and the necessity for V_{DS} compensation to ensure reliable performance.

A summary of prior art was presented, demonstrating that existing solutions require a significantly larger chip area, which limits their practicality. To overcome this limitation, two novel compensation techniques have been developed: I_{ref} and I_{vgs} methods. Based on these, two new circuit architectures have been designed without a significant increase in chip area. One of these architectures, based on the I_{ref} compensation has been implemented in silicon, with measured results closely matching the simulated ones, demonstrating the excellent performance of the proposed solution. Both approaches were included in a patent application [14].

The proposed solutions effectively reduce the charge current error from 25% to 2%, showcasing their potential for improving the precision and reliability of gate drivers in practical applications. Due to their proven effectiveness in reducing charge current error, these methods are strong candidates for integration into future high-performance gate driver products.

Acknowledgement. The authors would like to thank Infineon Technologies for the support, encouragement of new ideas, and openness to implementing them in new products. Additionally, the results of this work would not have been possible without the support and technical expertise of Cristian Murtaza, Dragos Panaite and Ansgar Pottbaecker.

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