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The Force Extraction Concept with Application to Power IGBTs

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Abstract. A practical approach to speed up the turn-OFF of a power semiconductor which employs conductivity modulation of the drift region is presented. The concept proposed, named Forced Extraction, involves accessing the region where the injection of the minority carriers takes place via an Extraction Plug. This path is connected to an Extraction Device that will remove excess carriers during switch turn-OFF. Validation of the Forced Extraction concept is performed for IGBTs, whose long turn-OFF tail limits their high-frequency functionality. SPICE, TCAD and mixed-mode simulations in the case of a very small in size Extraction Device (lateral *p*MOS) show reductions of turn-OFF energy by up to 40%. Furthermore, efficiencies of over 98% at 25 kHz are achieved in three-phase inverters using IGBTs with these Forced Extraction mechanisms.

Key-words: Extraction device; extraction plug; IGBT; switching behavior; turn-OFF energy.

1. Introduction

The field of power semiconductor devices is currently extremely active, driven by the rapidly emerging Green Energy field [1-3]. Solar power, automotive, energy grid, aerospace applications, Internet (data centers) constitute just an abridged list of "application spaces" for power semiconductor components, for which the demand for higher efficiency, better reliability, smaller and heat capable packages trigger intense development efforts across the entire community of suppliers [4-6].

Among these devices, the Insulated Gate Bipolar Transistor (IGBT) stands out as the most commercially advanced, seamlessly combining the high-input impedance MOS-gate control with the efficient bipolar current conduction that minimizes forward voltage drop [7-9]. This unique combination not only enhances performance but also simplifies circuit design, reducing both the size and complexity of the controlling circuitry [10]. As a result, IGBTs contribute significantly to cost reduction and improved efficiency in various power electronic applications. The layout of vertical IGBTs, where the main electrodes are on opposite sides of the structure, is conductive to high currents, high voltage and therefore high-power dissipation [11]. In such applications, the addition of a freewheeling diode (FWD) becomes mandatory. Conversely, IGBTs are not well-suited for high-frequency applications primarily due to their slow turn-OFF characteristics, which are limited by the recombination of excess carriers in the base [7]. When the IGBT is turned OFF, the stored minority carriers must decay through recombination, a process governed by the carrier lifetime [12].

Several techniques have been proposed to speed up the turn-OFF time of the IGBT [13], either by a reduction in the minority-carrier lifetime or by falling the injection efficiency of the IGBTs emitter junction.

To address the turn-OFF limitation of power semiconductors employing conductivity modulation in the drift region, in this paper, a practical approach called Forced Extraction (FE) will be explored. The idea was initially proposed for a complementary IGBT structure, with an integrated *p*MOS that drew excess carriers out [14], [15]. By accelerating the recombination process, this method significantly improves the turn-OFF speed, making power devices more suitable for high-frequency applications while maintaining their advantages in efficiency and cost-effectiveness. Our study investigates different ways of implementing an Extraction Plug (access electrode), which enables direct access to the region where minority carrier injection occurs, for a more efficient removal of excess carriers without compromising the blocking capability of the device [16], [17].

The FE concept is implemented on IGBT power devices (FE-IGBT). Two possible approaches are investigated [16], [17]. Firstly, an integrated FE-IGBT, for which the Extraction Plug and the Extraction Device (a lateral *p*MOS transistor with thick gate oxide) are built together on the same die. Secondly, a "hybrid" solution is proposed and explored, with the *p*MOS Extraction Device [18] integrated onto the freewheeling diode (FWD) instead.

This paper is organized as follows: the Forced Extraction concept is presented in Section 2 with aspects regarding its implementation on IGBT power device described in Section 3. The validity of this approach and its benefits are achieved by SPICE, TCAD and mixed-mode simulations in Section 4. Section 5 illustrates simulations and energy efficiency evaluations on a three-phase traction inverter for Electric Vehicles.

2. Forced Extraction Concept

The concept of Forced Extraction [19] applies to any power switch, such as the IGBT, bipolar transistor or thyristor, with conductivity modulation of the drift layer (the part of the device that withstands the voltage). If the drift layer of the power device is crowded with minority carriers, their removal will take time, degrading the switching speed, lowering the frequency of operation and increasing the turn-OFF energy [20].

The concept was first presented by Boisvert and Plummer [14], but their implementation was not suited for modern, high-voltage IGBTs. Their proposed device was based on a vertical IGBT, with an integrated *p*MOS transistor, contacting the IGBT drift region via an n^+ diffusion, through a break in the polysilicon gate. The *p*MOS transistor provides a path for carriers to the reach positively biased drain of the IGBT, without causing back injection into the base region [14]. This implementation was limited to applications under $100V$, with no additional efforts to adapt the idea for high-voltage power switches.

This paper aims to expand this concept for high-voltage applications using IGBTs.

Figure 1 depicts the fundamentals of the FE concept: A Main Switch with built-in Extraction Plug (EP), accessing the region of the switch whence the minority carriers need to be removed, is connected to an Extraction Device (Figure 1). This device (M2 - Figure 1b) has its control and output terminals joined to the input and output pins of the main switch (IGBT, comprising M1 and Q - Figure 1b), respectively. The Extraction Plug (Figure 1a) should not degrade the blocking, high temperature and long-term reliability capabilities of the overall power switch, the FE-IGBT.

Table 1 summarizes the operation of the FE switch. When the Main Switch is in the ON state, the Extraction Device should be OFF, so as not to influence conduction functionality. When the main switch turns OFF, the Extraction Device should be ON and provide a conduction path for

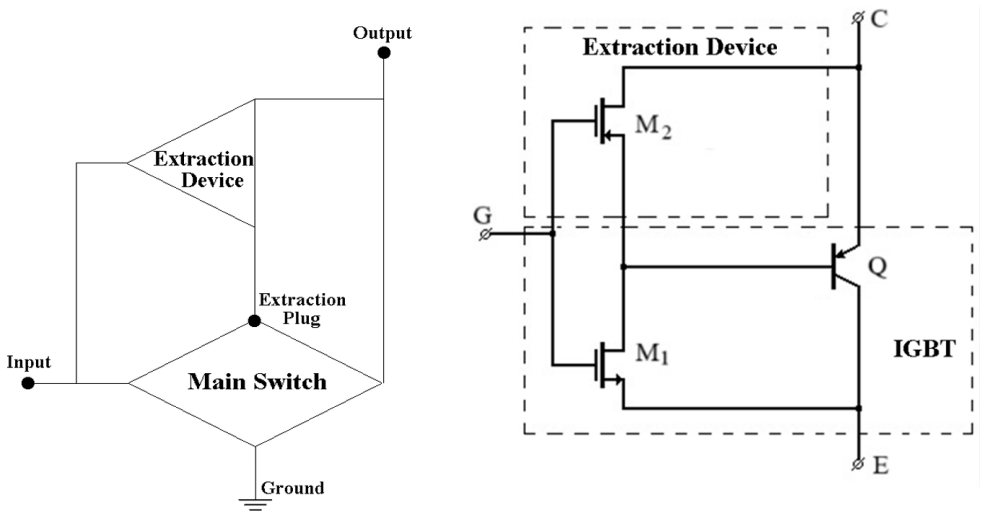

Fig. 1. a) Generic circuit of the Forced Extraction Concept [18] and b) electrical schematic of the FE-IGBT.

Table 1. Operational States of Main Switch and Extraction Device

Device/State	Turn-ON	Turn-OFF	Input Voltage	Output Voltage
Main Swaich	ON	OFF	Low	High
Extraction Device	OFF	ON	High	Low

carriers to be removed from the drift region. Thus, a significant turn-OFF time reduction is achieved, lowering energy losses and improving operating frequency.

The trade-off between the size of the Extraction Device and the reduction of the turn-OFF energy has to be carefully considered. The FE-IGBT implementation will create a three terminal device, fully compatible with the generic IGBT.

3. FE-IGBT Implementation

The implementation of the FE-IGBT has different options:

- Integrating the *p*MOS Extraction Device with the IGBT structure (similar to [14]). In order to extend voltage capability, either a thick gate oxide for the *p*MOS should be developed, or a high-voltage capacitor can be placed between the gates of the Main Switch and Extraction Device. Since the latter option entails a more complex assembly process, the implementation costs are higher. As such, employing an extraction pMOS with thick gate oxide is generally preferable.
- Integrating the Extraction Device with the freewheeling diode (FWD). The FWD is mandatory for the protection of the IGBTs that work on inductive loads. Lumping these two blocks together represents a versatile solution, as both devices need to withstand the full voltage range of the overall power switch (FE-IGBT).

Both cases require adequate terminations in order to ensure high-voltage capabilities. In the case of a vertical power semiconductor, the layout of the p-wells determines the shielding of the M2 gate oxide (Figure 1b). Figure 2a illustrates the cross section of a FE-IGBT having a deep trench termination and integrated *p*MOS Extraction Device. The distribution of current flow-lines (Figure 2a) is strongly impacted by this layout. Current conduction takes place preferentially through the plug toward the *p*MOS, during its ON operation. The EP, together with the Extraction Device represent the foundation of the Forced Extraction technique.

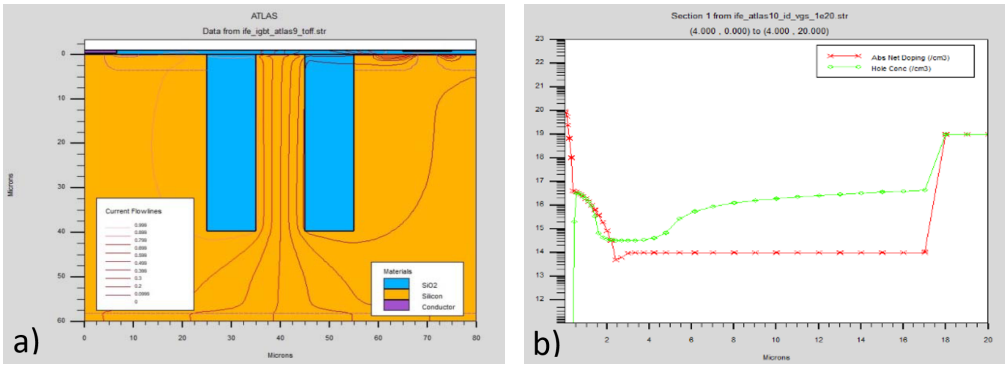

Fig. 2. a) Cross-section of a vertical FE-IGBT with integrated *p*MOS Extraction Device and b) TCAD hole carrier distribution simulation.

The Extraction Plug represents the access path to the drift layer of the IGBT. In order to effectively remove minority carriers from this region, their distribution needs to be considered. It is observed that the carrier concentration is higher toward the bottom end of the drift layer (Figure 2b). This is an essential aspect when considering the EP positioning and depth (Figure 2a).

There are three ways of placing Extraction Plugs inside of the IGBT die, which ensure electrical access to the drift region:

- A trench, tailored to withstand blocking voltages in excess of the voltage rating of the power switch (Figure 2a).
- A planar high-voltage termination surrounding a small n^+ island, contacting the drift region in-between the IGBT gate, similar to [14].
- An n^+ ring, placed outside of the high-voltage termination of the IGBT, but properly designed to accommodate the device's maximum ratings.

Out of these possibilities, the trench implementation is preferred, due to the carrier distribution observed in the TCAD simulations. Since the hole concentration is higher towards the end of the drift layer (Figure 2b), a deep trench EP is recommended, in order to properly access and extract these carriers.

4. Results

The FE-IGBT functionality was analyzed by SPICE, TCAD and mixed-mode simulations, in comparison with a standard IGBT. There are a multitude of SPICE models for IGBTs, with varying degrees of complexity. In our simulations, we have used the model from [21], with parameters specific to the Fuji IGBT (FGZ75N65WE), as the generic comparison device. This model was adapted to a FE-IGBT structure by implementing an extraction device, as shown in Figure 3.

Q1 is the equivalent pnp transistor of the IGBT and its base is, in fact, the drift layer whence the minority carriers need to be extracted.

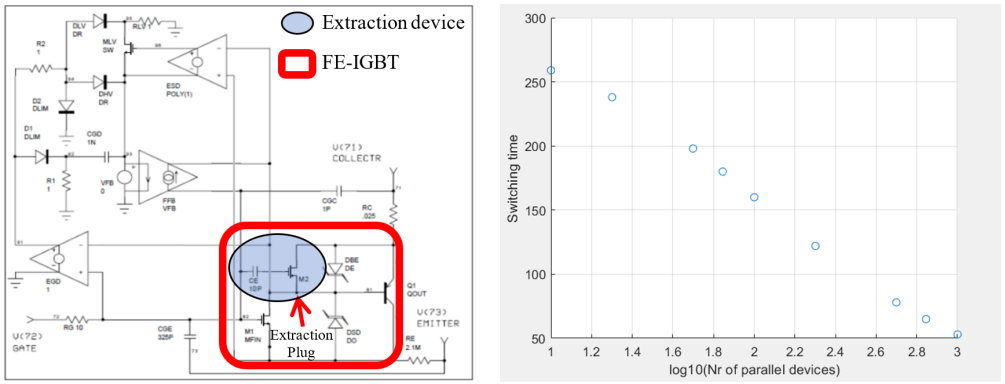

Fig. 3. a) Spice model of a power IGBT [21] with added Extraction device and b) Turn-OFF switching time vs. the number of *p*MOS transistors.

For the sake of optimizing the cost of the FE-IGBT, by minimal changes to the process flow and controlling electromagnetic interference, a Linear 3N163 *p*MOS transistor was selected for M2 (Figure 3a). The capacitor CE was added between the gates of M1 and M2 (Figure 3a) in order to ensure that the maximum voltage ratings of the *p*MOS are not exceeded during IGBT switching. Figure 3b depicts the reduction in switch-OFF time versus M2 multiplicity. A logarithmic dependence can be observed, indicating that even low Extraction Device lengths can significantly improve FE-IGBT switching capabilities.

Table 2 presents a comparison between standard and FE-IGBT in terms of ON voltage ($V_{CE,on}$), threshold voltage (V_{Th}), blocking current (I_{CES}) and main gate charges. Adding a small size Extraction Device does not deteriorate these essential IGBT electrical parameters. The switching behavior on both inductive and resistive loads was assessed further for these two power switches. Figure 4 presents SPICE simulations for turn-OFF energy as a function of $V_{CE,on}$. This voltage was modified by adjusting the current gain of the pnp transistor. A significant decrease in energy loss, up to 40%, is observed for the FE-IGBT, in both switching cases (Figure 4).

An important conclusion following this analysis is that the Extraction Device enables a considerably higher injection level for the pnp emitter, which leads to a decrease in ON-state resistance or facilitates smaller IGBT die sizes (with associated improvement in cost and switching speed).

Switching behavior was assessed also via TCAD mixed-mode simulations, with the setup presented in Figure 5. A FE-IGBT structure with a Deep Trench Extraction Plug and a lateral *p*MOS with thick gate oxide were considered (Figure 5a). In these simulations, the interdigitated (comb) design of the main IGBT has a channel width equal to $200cm$, with a die size about $25mm^2$, typical of a power IGBT ($650V$). The channel width of the *p*MOS simulated was equal to $1cm$ (very small size compared to the overall IGBT die).

Figures 6 and 7 present the output current, voltage and switching power for an IGBT with only EP versus its complete FE-IGBT counterpart, respectively. The turn-OFF speed of the FE-IGBT is noticeably faster. Consequently, the energy losses are lower. An E_{OFF} reduction of approx. 40% was calculated from power characteristics (Figures 6c and 7c), in agreement with SPICE simulations (Figure 4). Furthermore, Figure 6d confirms that the Extraction plug generates an insignificant leakage current. When an Extraction Device is connected, its current

Table 2. Comparison between main Electrical Parameters of Standard and FE-IGBT

Device	$V_{CE,on}$ @$90A$	V_{Th} $(1mA)$	I_{CES} $(600V)$	Q_{GE} $(400V, 50A)$	Q_{GC} $(400V, 50A)$	Q_{tot} $(400V, 50A)$
Standard IGBT (FGZ75N65WE)	$1.9\ V$	$4\ V$	$640\ \mu A$	$87\ nC$	$156\ nC$	$330\ nC$
FE-IGBT	$1.9\ V$	$4\ V$	$690\ \mu A$	$88\ nC$	$157\ nC$	$335\ nC$

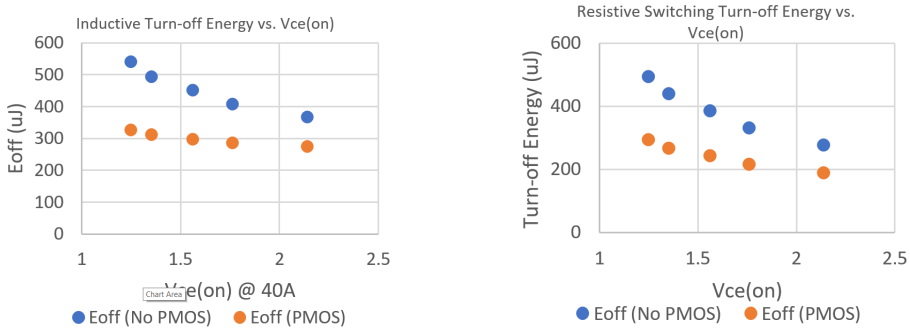

Fig. 4. a) Inductive Turn-OFF Energy vs. On Voltage and b) Resistive Turn-OFF Energy vs. On Voltage (FE-IGBT vs. Std. IGBT).

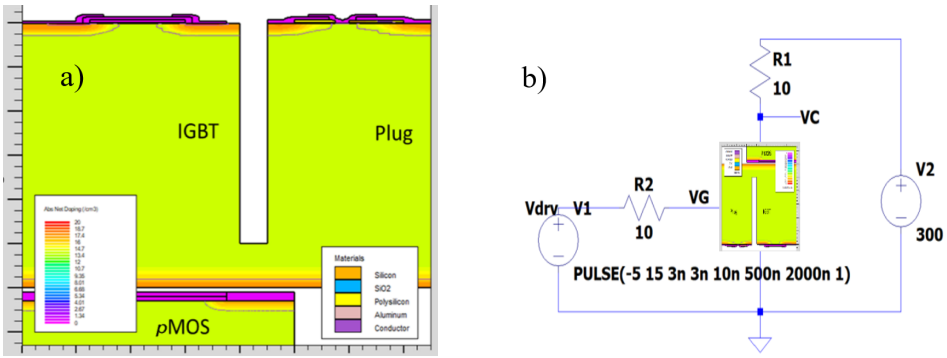

Fig. 5. a) FE-IGBT cross-section with separate *p*MOS Extraction Device and b) Mixed-Mode TCAD simulation setup.

flows fully through the EP (Figure 7d).

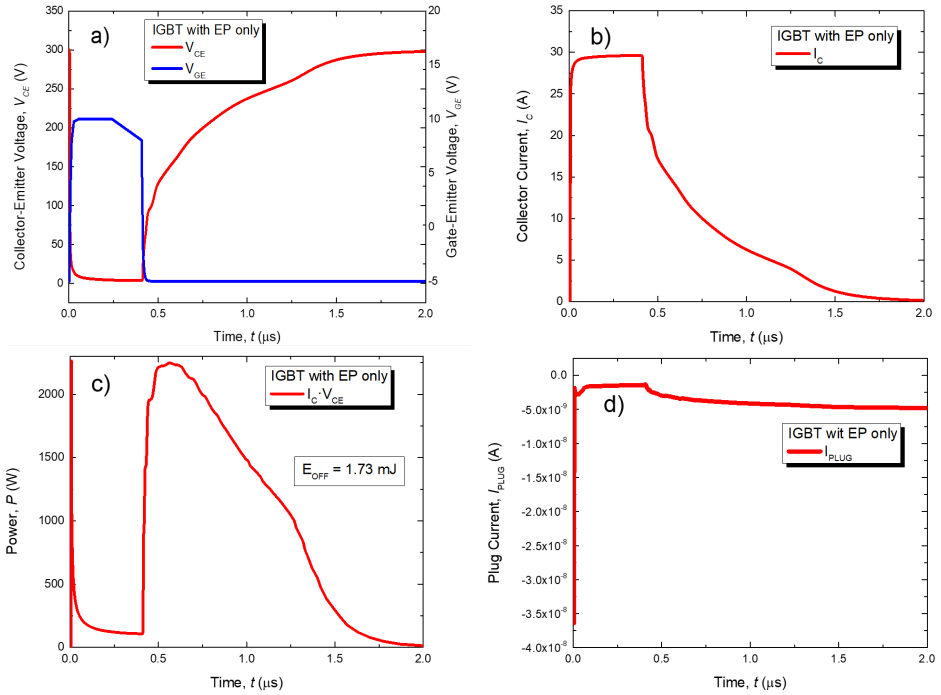

Fig. 6. Resistive switching simulations for IGBT with EP only: a) output voltage (V_{CE}), b) collector current (I_C), c) output power and d) extraction plug current.

The spikes of the plug current, visible in Figure 7d, are due to the ramp-up times of the input signal (V_{GE} - Figures 6a and 7a). To illustrate the case where the FE-IGBT's Extraction Device is integrated with its freewheeling diode, Figure 8 depicts TCAD cross-section simulations. This FWD-Extraction Device tandem was implemented on silicon carbide (SiC) [22], [23] in order to ensure adequate high-voltage capabilities.

The presence of the Extraction Device does not influence the normal operation of the FWD during its ON state, as most of the anode current flows only through the diode, as shown in Figure 8b.

The comprehensive simulation results presented above strongly indicate that the Forced Extraction Concept can be successfully applied to IGBTs in order to reduce switching energy and improve operation frequencies.

5. Applications

Power IGBTs are typically used in inverters for automotive applications [24]. A simple, generic, three-phase inverter circuit, depicted in Figure 9a, was selected in order to evaluate efficiency improvements yielded by using the FE-IGBT.

The main control switch in the circuit was, alternately, the Fuji IGBT and the FE-IGBT (a same-power IGBT with an Extraction Plug and 3N163 *p*MOS extraction transistor - see Fig-

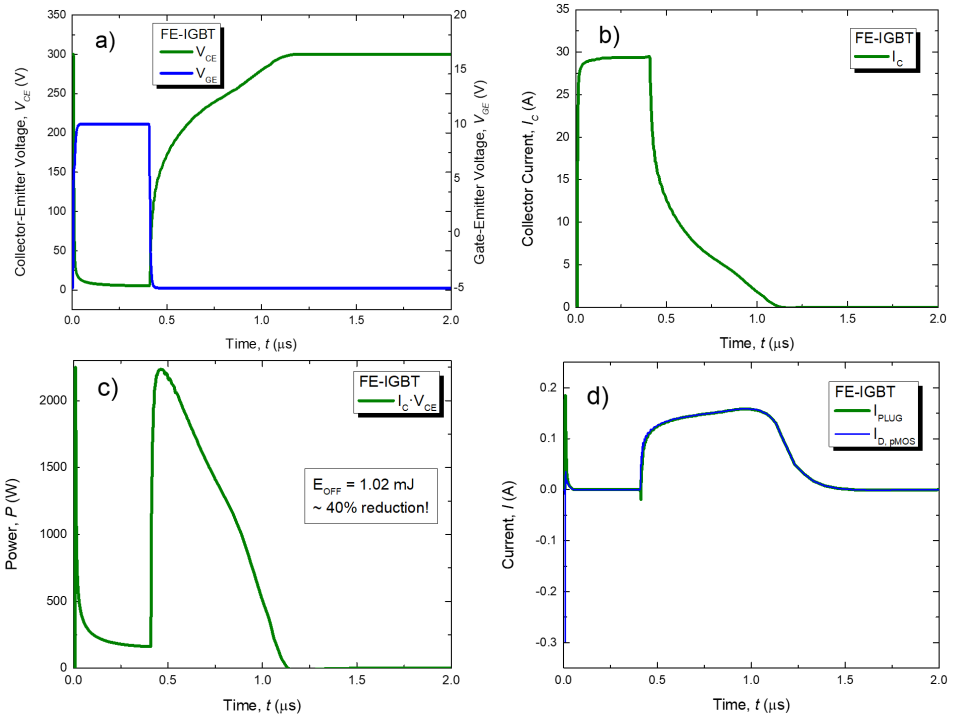

Fig. 7. Resistive switching simulations for FE-IGBT (IGBT with Extraction Device connected to EP): a) output voltage (V_{CE}), b) collector current (I_C), c) output power and d) extraction currents.

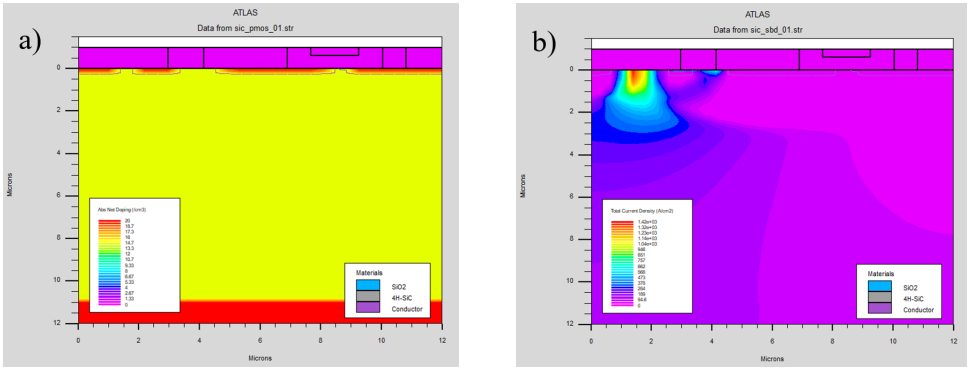

Fig. 8. Cross section of a) an integrated SiC freewheeling diode and *p*MOS Extraction Device and b) anode current flow through the FWD.

ure 3a). Circuit operation is validated by Figure 9b waveforms, showing the proper phase shift between output current phases.

Power loss of the switches and the efficiencies of the three-phase inverters are plotted in Figure 10. As the switching frequency increases, the superiority of the FE-IGBT in this application becomes evident, with almost 1 percentage point above the value of 97.5% efficiency of the standard IGBT (at 25 kHz).

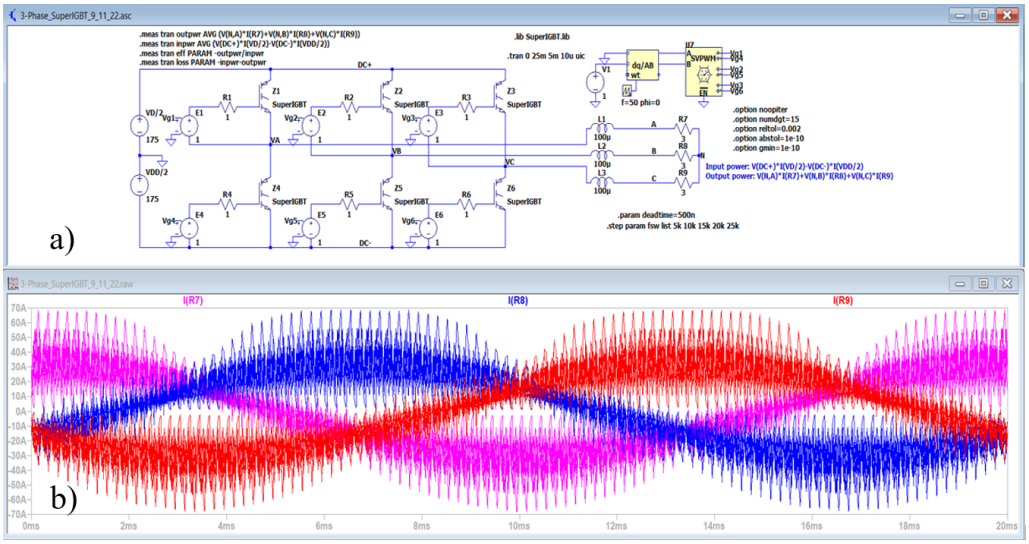

Fig. 9. Three Phase Inverter with IGBT as the main control switch: a) SPICE schematic and b) typical output current waveforms for each phase.

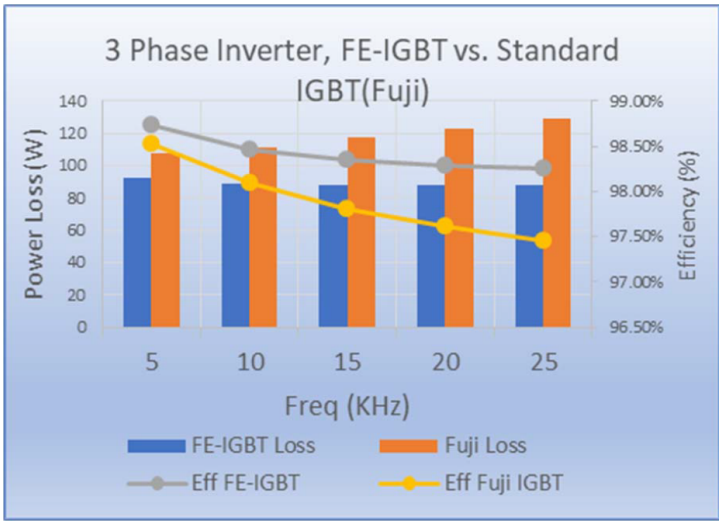

Fig. 10. Spice Simulations of a Three Phase Inverter.

6. Conclusions

In this paper, a viable implementation of the Forced Extraction concept was presented. This solution is catered to power IGBTs, via the addition of a Deep Trench Extraction Plug, connecting to a *p*MOS Extraction Device. Thus, a mechanism to remove excess minority carriers from the drift layer is established. From general aspects of the concept, a realistic design of a Deep Trench Extraction Plug was performed on power IGBT switches. Also, two approaches were considered for Extraction Device integration, either directly with the IGBT, or together with the freewheeling diode. The FE-IGBT performances were validated by SPICE, TCAD and mixed-mode simulations. It was evinced that neither the EP nor the Extraction Device degraded the overall IGBT electrical behavior. Conversely, notable improvements in turn-OFF speed and energy efficiency, up to 40% during switching, were recorded. Furthermore, simulations on a three-phase inverter automotive application with FE-IGBTs yielded spectacular efficiencies, over 98% at operating frequencies up to 25 KHz.

The FE-IGBT has a significantly better trade-off between blocking and conduction performances, translating into a better technology curve. If properly implemented, this solution will revive the IGBT marked for the foreseeable future.

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