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Impact of Scaling and Interface Roughness on Drain Current in Nanosheet and Nanowire FETs: A 3D Monte Carlo Analysis

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Abstract. A 3D finite-element Monte Carlo simulation toolbox, incorporating Schrödinger equation-based quantum corrections, is employed to analyze the performance of nanosheet (NS) and nanowire (NW) field-effect transistors (FETs), which emerged as promising candidates for sub-3 nm CMOS technology. The study investigates the impact of scaling gate length and oxide thickness, increase in source/drain doping concentration, and interface roughness on these architectures. Results indicate that NS-FETs achieve higher ON currents than NW FETs. However, scaling the gate length below 12 nm reduces the drain current in both devices with a $\langle 110 \rangle$ channel orientation—by 9.4% in NS and 7.7% in NW. To understand this decline, valley population and average electron velocity are examined. Scaling dielectric thickness has a smaller effect on NW-FETs with 12 nm and 10 nm gate lengths compared to NS-FETs. In contrast, changes in maximum doping concentration have a greater impact on NW than NS, due to better electrostatic control and increased carrier injection resulting from reduced source/drain resistance. A back-scattering effect is observed in the 12 nm and 10 nm gate length devices, particularly NWs, but it can be mitigated by increasing doping concentration. Interface roughness significantly degrades drain current (I_{DD}), with a more pronounced impact on NWs. Their smaller surface-to-volume ratio and stronger quantum confinement increase sensitivity to roughness variations, as most carriers are closer to the surface, leading to more scattering events. On the contrary, NSs, despite interface roughness, benefit from a larger conductive cross-section, maintaining higher effective mobility in the device channel.

Key-words: Gate-All-Around; Monte Carlo; nanosheet; nanowire; scaling.

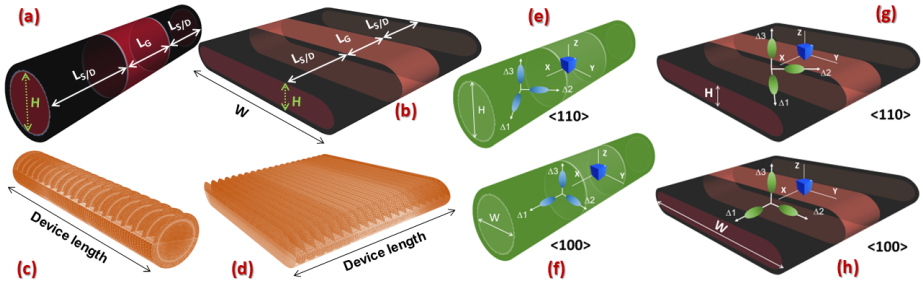

Fig. 1. Schematic 3D representation of (a) a nanowire (NW) FET and (b) a nanosheet (NS) FET, highlighting key dimensions: width (W), height (H), gate length (L_G), and source/drain length ($L_{S/D}$). (c, d) 2D cross-sections of the 3D finite element (FE) mesh for the NW (left) and NS (right) device channels, used in the Schrödinger equation solver. (e–h) Δ-valley positions for different channel orientations: (e) NW-FET with $\langle 110 \rangle$, (f) NW-FET with $\langle 100 \rangle$, (g) NS-FET with $\langle 110 \rangle$, and (h) NS-FET with $\langle 100 \rangle$.

1. Introduction

Gate-all-around (GAA) nanosheet (NS) and nanowire (NW) FETs represent the next architectural evolution in FET technology, addressing the limitations of FinFET designs [1]. GAA-FETs exhibit several advantageous characteristics, including vertical three-dimensional (3D) stacking [2, 3], reduced power-consumption, enhanced drive-current, increased device-density, and improved electrostatic-control. Additionally, they demonstrate superior immunity to short-channel effects and are well-suited for integration into sub-3 nm technology nodes [4]. Their excellent gate controllability positions them as a promising candidate for continued transistor scaling and performance optimization in advanced semiconductor technologies [5]. Achieving a larger drain current is essential for improving the switching speeds of GAA-FETs. Still, the drain current increase remains a significant challenge due to a contradictory requirement of the gate control [6]. While stacking techniques improve drain current in GAA-FETs [7], they introduce fabrication challenges such as irregular sheet dimensions, doping variations, and elevated device temperatures. Moreover, the efficiency of stacked NS diminishes beyond three layers [8], [9]. This work investigates the effects of scaling the gate length (L_G), reduction of equivalent oxide thickness (EOT), increase in maximum doping concentration (MDC), and change in interface roughness (IR) on NS-FETs and NW-FETs (see Fig. 1) using state-of-the-art, in-house developed, 3D ensemble Monte Carlo (MC) device simulations [6, 10].

2. 3D Ensemble Monte Carlo Simulation

This simulation study explores strategies to enhance the electrical performance of n-type NS-FETs and NW-FETs (see Fig. 1) at sub-2 nm technology nodes by examining the gate length scaling (L_G), high-κ dielectric layer thickness, maximum doping concentration (MDC) in the source/drain (S/D) regions, and interface roughness (IR) between the channel and dielectric layer

Table 1. Device and material parameters for both NS-FETs and NW-FETs. The thickness of high-κ dielectrics is given as the equivalent oxide thickness (EOT)

Energy Difference for Si Δ-Valleys in TB (NW) Compared to Bulk (NS)		
Device Type	NS	NW
Δ_x (E_{G1}-Δ_{x1}) [eV]	1.12	1.282
Δ_y (E_{G2}-Δ_{x2}) [eV]	1.12	1.247
Δ_z (E_{G3}-Δ_{x3}) [eV]	1.12	1.247
Dimensions and Parameters	NS	NW
Height (H) [nm]	5	7.17
Width (W) [nm]	50	5.7
Perimeter (P) [nm]	110	20.28
S/D region length ($L_{S/D}$) [nm]	14	14
Uniform p-type channel [cm^{-3}]	1×10^{15}	1×10^{15}
Channel orientation	$\langle 110 \rangle, \langle 100 \rangle$	$\langle 110 \rangle, \langle 100 \rangle$
High-κ thickness (EOT) [nm]	1.0, 0.9, 0.8	1.0, 0.9, 0.8

in order to meet the demands of sub-2 nm technology nodes. Given the highly non-equilibrium transport regime at on-current in these FETs, an ensemble MC technique with Schrödinger equation (SchEq) quantum corrections must be used to account for quantum confinement and scattering, especially in shrinking GAA-FET channels. The simulations employ an in-house finite element (FE) toolbox with a 3D tetrahedral mesh to accurately describe the shape of a nanoscale device. For quantum corrections, the toolbox incorporates 2D SchEq solutions on channel slices embedded into the 3D mesh, as illustrated in Fig. 1(c) and (d). A key advantage of SchEq-based quantum corrections is eliminating the need for calibration, unlike the density-gradient (DG) method, which requires extensive mass fitting [11]. In the subthreshold region, where diffusion transport dominates, the drift-diffusion (3D-DD) transport method is used under low gate biases. At higher gate biases, where non-equilibrium effects dominate, the 3D-MC method accurately models the ON region. The MC simulation uses 200,000 particles, with 60,000 initially assigned to contacts, using a time step of 0.05 femtoseconds. The work function is set to 4.3 eV, and the channel is divided into 20 perpendicular slices for quantum corrections. The MC engine includes all Si-relevant scattering mechanisms such as phonon scattering, ionized impurities, and IR scattering within an anisotropic non-parabolic bandstructure considering X, L, and Γ valleys [13].

To investigate the effects of dielectric layer thickness, MDC, and IR, we first validate the simulation tool against experimental data from an IBM-fabricated NS-FET [12]. As shown in Table 1, the nanosheet has a gate length (L_G) of 12 nm, a thickness of 5 nm, and a width of 50 nm. The high-κ dielectric layer made of hafnium dioxide (HfO_2) has an equivalent oxide thickness (EOT) of 1 nm. Since a specific doping profile (DP) is typically unknown, we employed a reverse engineering approach based on our previous methodology [14] to approximate the doping profile by Gaussian shape. The Gaussian doping profile parameters are set to $x_{max} = 11.3$ nm and $x_{char} = 3.45$ nm, with an MDC of $5 \times 10^{19} cm^{-3}$. IR scattering is characterized by an RMS height (Δ_{rms}) of 1.5 nm and a correlation length (λ_{cl}) of 1.7 nm and are obtained from experimental data [15]. Fig. 2 shows an excellent agreement of I_D-V_G characteristics obtained from the MC simulations with experimental data [12]. The accuracy of the toolbox for NS-FETs and NW-FETs has been also validated in many previous studies [16], [17], [6], [18].

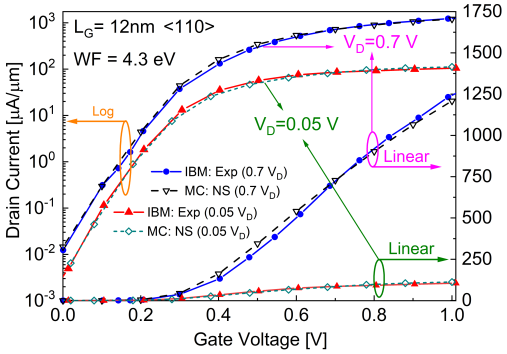

Fig. 2. I_D-V_G characteristics at high and low drain biases for a 12 nm L_G NS-FET, compared with experimental data [12], demonstrating the validation and accuracy of the toolbox.

3. I-V Characteristics of Nanosheet and Nanowire FETs

In this section, we explored our findings in detail for the studied devices (NS and NW FETs).

3.1. Gate length scaling

Following validation depicted in Fig. 2, NS-FETs, and NW-FETs with two channel orientations, $\langle 110 \rangle$, and $\langle 100 \rangle$, are analyzed assuming an EOT of 1.0 nm and an MDC of 5×10^{19} cm^{-3}. Subsequently, both device orientations with the 12 nm gate length were further scaled to 10 nm (L_G), aligning with IRDS guidelines for future technology nodes [19]. The NW transistor is modeled with an elliptical cross-section to account for fabrication-induced etching effects [20]. Since the nanowire (NW) transistor has a small cross-section (longer diameter: 7.17 nm, shorter diameter: 5.7 nm), its band structure is significantly influenced by quantum-mechanical confinement effects and cannot be approximated as a bulk band structure [21]. Therefore, the tight-binding (TB) method is employed to determine the band structure in **k**-space, from which the electron effective masses are extracted (see Table 1). To ensure a fair comparison, currents are normalized to the device perimeter: the NS-FET had a perimeter of 110 nm, while the NW-FET had a perimeter of 20.28 nm. The drain drive current (I_{DD}), representing the current flowing in

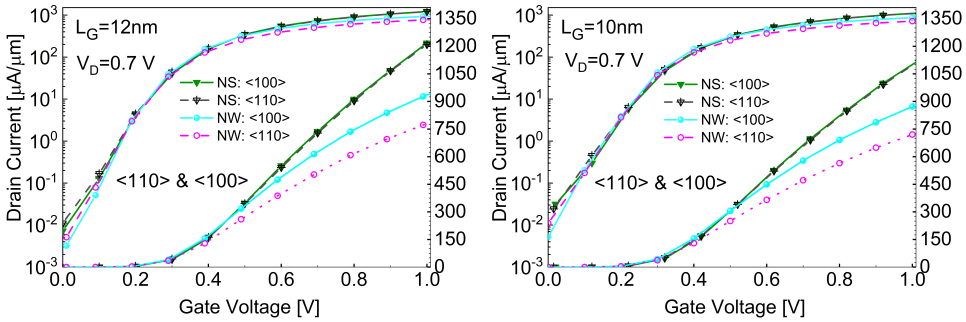

Fig. 3. The simulated I_D-V_G characteristics at a high drain bias of 0.7 V for the 12 nm (left) and 10 nm (right) L_G NS-FETs and NW-FETs with channel orientations $\langle 110 \rangle$ and $\langle 100 \rangle$.

the channel when the transistor is in the ON-state, is obtained at $V_G - V_T$ and $V_D = 0.7$ V. As illustrated in the Fig. 3, with $\langle 110 \rangle$ channel orientation, the devices with a 12 nm L_G exhibit higher drain drive currents (I_{DD}) compared to their scaled counterparts with a 10 nm L_G, for both NS-FETs and NW-FETs. Specifically, the 12 nm L_G NS-FET achieves $I_{\mathrm{DD}} = 1065\ \mu\mathrm{A}/\mu\mathrm{m}$, while the 10 nm L_G NS-FET achieves $I_{\mathrm{DD}} = 965\ \mu\mathrm{A}/\mu\mathrm{m}$. Similarly, the 12 nm L_G NW-FET achieves $I_{\mathrm{DD}} = 704\ \mu\mathrm{A}/\mu\mathrm{m}$, compared to $I_{\mathrm{DD}} = 650\ \mu\mathrm{A}/\mu\mathrm{m}$ for the 10 nm L_G NW-FET, as illustrated in Fig. 3 The reduction in drain current with gate length scaling is primarily due to decreases in the number of electrons injected into the channel. This is caused by the effects of Fermi-Dirac statistics in the n-type doped S/D regions, as the fringing electric field increases with gate scaling at the source side of the gate. The increased electric field leads to back-scattering towards the source, resulting in a reduction in electron injection. The reduced injection, in turn, leads to a lower overall electron density in the channel. This decrease in electron density ultimately leads to a reduction in the I_{DD} of scaled devices [6]. Further investigation is conducted to understand the physical mechanisms underlying device behavior and confinement effects, focusing on the impact of valley populations on the total drain current.

3.1.1. Effect of confinement and valley population

This subsection examines the valley population to assess its role in a quantum-confined channel, while the next subsection provides additional insights into the average electron velocity. The device orientations and corresponding conduction band energy ellipsoids for the Δ_1 (aligned with $\mathbf{k_x}$), Δ_2 (aligned with $\mathbf{k_y}$), and Δ_3 (aligned with $\mathbf{k_z}$) valleys in NW-FET and NS-FET channels are shown in Fig. 1. The $\langle 110 \rangle$ channel orientation is illustrated in Figures 1(e) and 1(g), while the $\langle 100 \rangle$ orientation is depicted in Figures 1(f) and 1(h). The longitudinal (m_l) and transverse (m_t) effective masses vary with transport direction, highlighting the significance of valley alignment in device performance. Figures 1(e) and 1(g) illustrate the Δ_1 and Δ_2 ellipsoids for devices with the $\langle 110 \rangle$ channel orientation, where m_t is not aligned with the transport direction (x-axis), reducing its contribution to the current. In contrast, Figures 1(f) and 1(h) show that for the $\langle 100 \rangle$ orientation, m_t of Δ_2 and Δ_3 aligns with the transport direction, leading to similar velocities and greater contributions to the drain current. Figures 4 and 5 illustrate the valley contributions to the total drain current for the 12 nm and 10 nm NS-FETs and NW-FETs, respec-

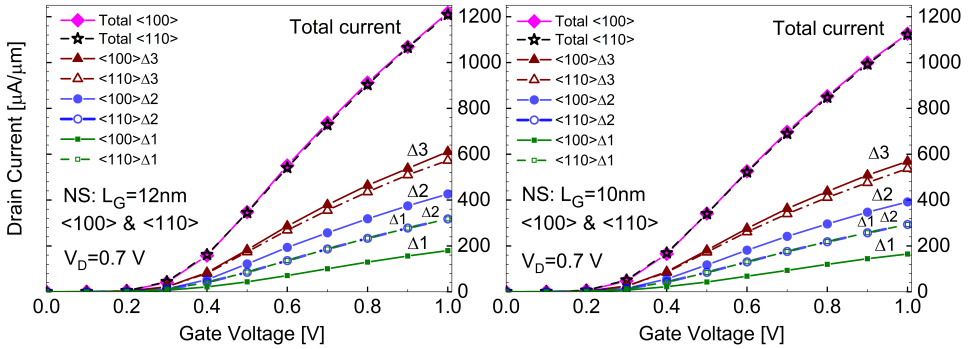

Fig. 4. Population of the Δ-valleys (refer to Fig. 1) contributing to the drain current at a high drain bias of 0.7 V for the 12 nm (left) and 10 nm (right) gate-length NS-FETs, shown for the two crystallographic channel orientations: $\langle 110 \rangle$ and $\langle 100 \rangle$.

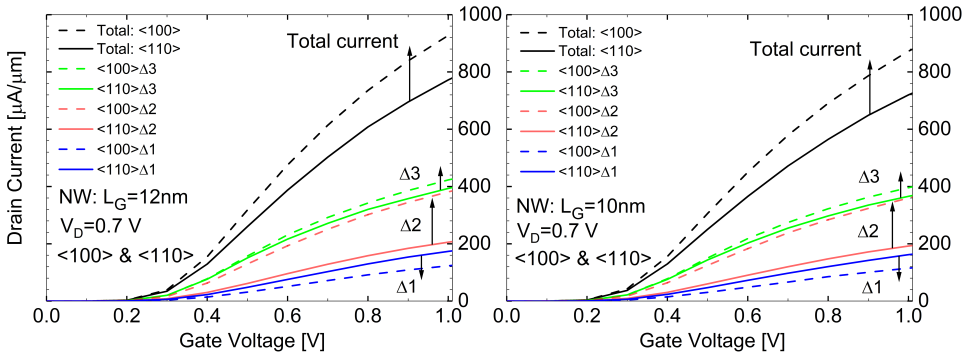

Fig. 5. Population of the Δ-valleys (refer to Fig. 1) contributing to the drain current at a high drain bias of 0.7 V for the 12 nm (left) and 10 nm (right) gate-length NW-FETs, shown for the two crystallographic channel orientations: $\langle 110 \rangle$ and $\langle 100 \rangle$.

tively, under a high drain bias of $V_{\mathrm{D}} = 0.7$ V. The 10 nm NS-FET exhibits a lower current than the 12 nm NS-FET. However, the impact of valley populations remains consistent across both the $\langle 100 \rangle$ and $\langle 110 \rangle$ orientations, despite the reduced gate length and changes in the exposed area under confinement control. In contrast, valley orientation is more pronounced in nanowires (see Fig. 5). For the $\langle 110 \rangle$ orientation, the drain current is reduced by 17% for the 12 nm device, and by 18% for the 10 nm device compared to the $\langle 100 \rangle$ orientation at $V_{\mathrm{G}} = 1.0$ V. This difference arises from the optimal confinement provided by the semi-circular shape of the NW-FETs, which enhances electron mobility in this orientation compared to the rectangular shape with rounded corners of the NS-FETs. Although the Δ_1 valley population in NW-FETs is larger in the $\langle 110 \rangle$ orientation than in the $\langle 100 \rangle$ orientation, this does not significantly increase drain current. The Δ_3 valley contribution behaves similarly for both gate lengths, with a slightly higher population in the $\langle 100 \rangle$ channel orientation. The Δ_2 valley contribution is smaller in the $\langle 110 \rangle$ orientation compared to the $\langle 100 \rangle$ orientation, resulting in a higher drain current in the NW-FET with the $\langle 100 \rangle$ orientation channel.

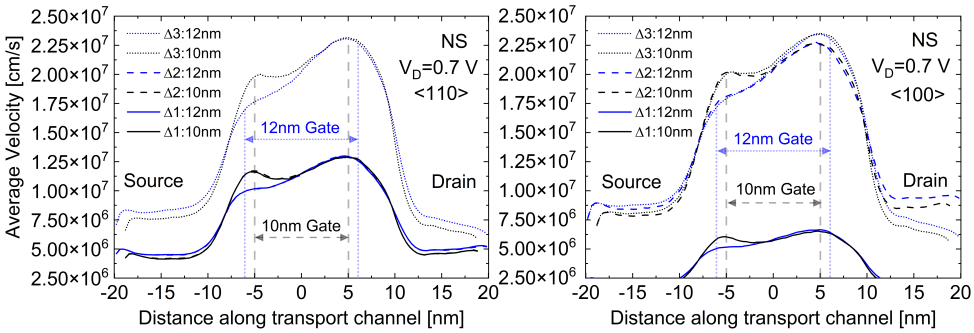

Fig. 6. The average velocity of electrons in the Δ-valleys along the channel is analyzed for the $\langle 110 \rangle$ (left) and $\langle 100 \rangle$ (right) orientations in the 12 nm and 10 nm gate length NS-FETs under the drain drive current (I_{DD}), defined at $V_{\mathrm{G}} - V_{\mathrm{T}}$ and $V_{\mathrm{D}} = 0.7$ V.

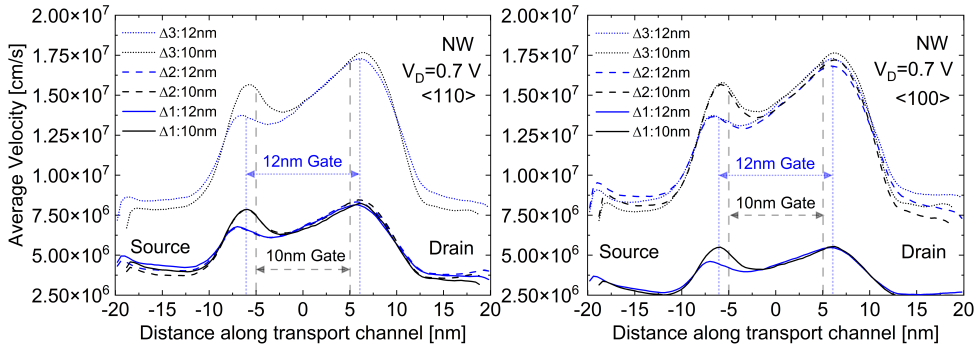

Fig. 7. The average velocity of electrons in the Δ-valleys along the channel for the $\langle 110 \rangle$ (left) and $\langle 100 \rangle$ (right) orientations in the 12 nm and 10 nm gate length NW-FETs under the drain drive current (I_{DD}), defined at $V_{\mathrm{G}} - V_{\mathrm{T}}$ and $V_{\mathrm{D}} = 0.7$ V.

3.1.2. Electron velocity in the device channel

Figure 6 presents the average electron velocity along the channel for the 12 nm and 10 nm L_G NS-FETs. In the $\langle 110 \rangle$ orientation (left), the Δ_3 valley (dotted lines) exhibits the highest average electron velocity due to its lighter effective mass, which significantly contributes to the total drain current. In contrast, the Δ_1 (solid lines) and Δ_2 (dashed lines) valleys contribute less because their heavier longitudinal effective masses (m_l) are in the transport direction. The dominance of transverse effective mass (m_t) in the Δ_3 valley accounts for its lighter effective mass compared to the heavier m_l of the Δ_1 and Δ_2 valleys (see Fig. 1). Similarly, Fig. 7 illustrates the average electron velocity along the transport channel for the NW-FETs ($L_G = 12$ nm and 10 nm). In the $\langle 100 \rangle$ orientation (right), the Δ_2 valley (dashed lines) shows a velocity comparable to that of the Δ_3 valley (dotted lines), while the Δ_1 valley, dominated by m_l, has the lowest velocity. This behavior is also observed in the $\langle 100 \rangle$ orientation of the NS-FETs in Fig. 6 (right). In the $\langle 110 \rangle$ orientation (left), the velocity of the Δ_2 valley approaches that of the Δ_1 valley, reducing its contribution to the current. Since the longitudinal mass, m_l, is heavier ($0.92\ m_0$, where m_0 is the free-electron mass), while the transverse mass, m_t, is lighter ($0.233\ m_0$), the Δ_2 valley plays a critical role in determining drain current due to its effective mass and alignment with the transport direction. In general, the average electron velocity gradually increases as it approaches the gate entrance. In the gate region, the electron is accelerated by the gate-induced fringing electric field and confinement effects, further increasing its velocity as it moves toward the gate-drain side. However, as shown in the figures, the average electron velocity decreases near the drain side due to significant scattering caused by the high doping impurity concentration in the drain.

3.2. Effect of thickness of high-κ dielectric layer

Fig. 8 illustrates the effect of reducing the thickness of high-κ dielectric layer for the 12 nm and 10 nm L_G NS-FETs. The real high-κ thickness is recalculated to the EOT using a respective dielectric constant. Starting with the 12 nm L_G NS-FET (left), when the EOT is reduced from 1 nm to 0.9 nm and further to 0.8 nm, I_{DD} increases by 4% (1107 μA/μm) and 9% (1159 μA/μm), respectively, compared to the 1 nm EOT result. Similarly, for the 10 nm L_G

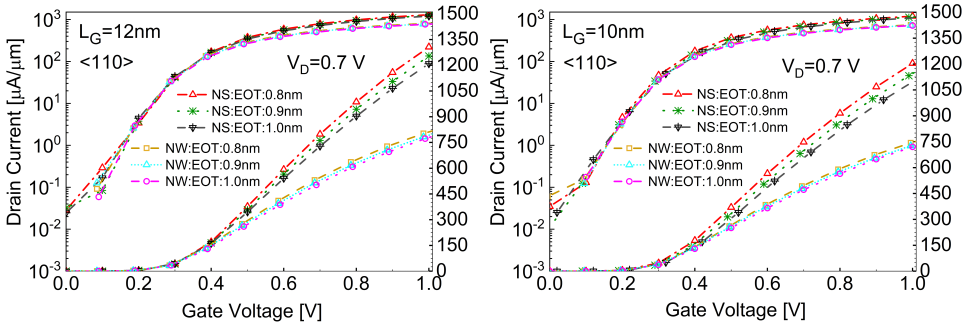

Fig. 8. Simulated I_D-V_G characteristics at a high drain bias of 0.7 V for the 12 nm (left) and 10 nm (right) L_G NS-FETs and NW-FETs with different EOTs.

NS-FET (right), I_{DD} improves by 5% (1015 $\mu A/\mu m$) and 10% (1068 $\mu A/\mu m$) compared to the 1 nm EOT result. For nanowires, reducing the EOT to 0.9 nm for the 12 nm L_G NW-FET results in a small increase (2%) in I_{DD} (718 $\mu A/\mu m$), while further reduction to 0.8 nm yields a 5% increase (740 $\mu A/\mu m$) compared to the 1 nm EOT result. Similarly, for the 10 nm L_G NW-FET, I_{DD} increases only by 1.5% (660 $\mu A/\mu m$) and 4.6% (680 $\mu A/\mu m$) with EOT reductions to 0.9 nm and 0.8 nm, respectively (see Fig. 8). These improvements are enabled by advancements in fabrication technology, such as the replacement of HfO_2 with materials like ZrO_2 or $HfZrO_2$ [22].

3.3. The effect of maximum doping concentration (MDC)

Adjustments to the MDC have a more pronounced impact on the on-current (I_{DD}) compared to the effects of EOT scaling for NS-FETs and NW-FETs, as presented in Fig. 9. When the MDC is increased from 5×10^{19} cm^{-3} to 1×10^{20} cm^{-3} and further to 2×10^{20} cm^{-3}, the 12 nm L_G NS-FET exhibits increase in the drain current of 19% (1265 $\mu A/\mu m$) and 29% (1370 $\mu A/\mu m$), respectively. On the other hand, the 12 nm L_G NW-FET shows even greater increase in I_{DD}, with improvements of 38% (975 $\mu A/\mu m$) and 72.7% (1216 $\mu A/\mu m$) at $V_G - V_T = 0.7$ V. For devices with a 10 nm L_G, increasing the MDC to 1×10^{20} cm^{-3} results in an I_{DD} improvement of 21%

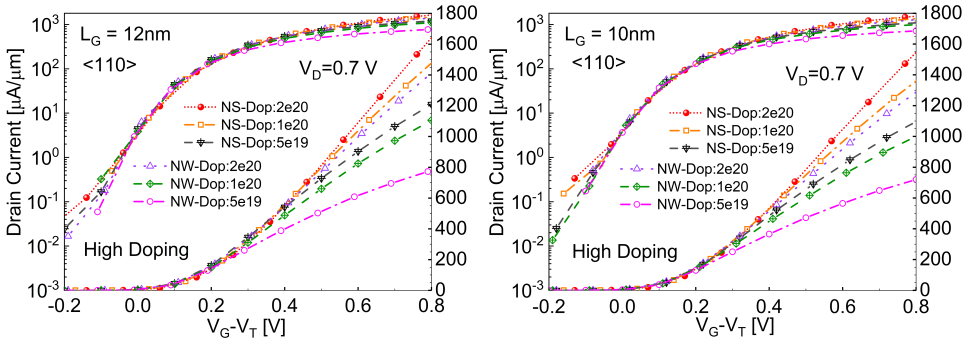

Fig. 9. Simulated I_D-(V_G-V_T) characteristics for 12 nm (left) and 10 nm (right) L_G NS-FETs and NW-FETs at a high drain bias of 0.7 V with different MDC values.

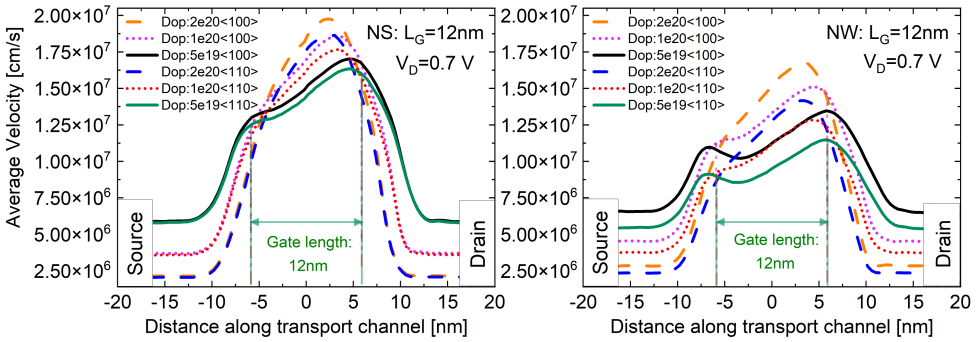

Fig. 10. Average electron velocity along the channel for 12 nm L_G NS-FETs (left) and 12 nm L_G NW-FETs (right) with $\langle 110 \rangle$ and $\langle 100 \rangle$ channel orientations at $V_{\mathrm{G}} - V_{\mathrm{T}} = 0.7$ V and $V_{\mathrm{D}} = 0.7$ V under different doping profiles.

(1170 μA/μm) for the NS-FET and 35.7% (882 μA/μm) for the NW-FET. Further increasing the MDC to 2×10^{20} cm^{-3} leads to even larger gains: 34% higher I_{DD} for the NS-FET and 67.7% higher I_{DD} for the NW-FET, as shown in Fig. 9. However, achieving such high MDC levels remains a significant technological challenge [23]. Nevertheless, the changes in the MDC inevitably alter the transistor threshold voltage (V_T). As a result, a fair comparison of transistor performance requires plotting the drain current as a function of (V_G - V_T) (the gate overdrive voltage), as illustrated in Fig. 9. While increasing the MDC enhances I_{DD}, it comes at the cost of a lower V_T, higher leakage current, increased scattering, and greater heat dissipation, all of which are detrimental to the performance of fast-switching devices. To better understand the impact of MDC on the drain current, we compare the average velocity of a 12 nm L_G NS-FET (left) and NW-FET (right) in Fig. 10, keeping the EOT fixed at 1.0 nm for all doping profiles. The NS-FET exhibits a higher average velocity, leading to a greater drain current compared to the NW-FET. For the $\langle 100 \rangle$ channel orientation, the highest peak velocity occurs at the largest doping, when the MDC profile is 2×10^{20} cm^{-3}, reaching approximately 2.0×10^7 cm/s, while the lowest value of the MDC profile (5×10^{19} cm^{-3}) results in about 1.7×10^7 cm/s—a 15% reduction. In contrast, the $\langle 110 \rangle$ orientation exhibits slightly lower velocities due to stronger quantum confinement effects. For the NW-FET, the highest peak velocity in the $\langle 100 \rangle$ orientation reaches 1.67×10^7 cm/s at the largest doping and 1.35×10^7 cm/s at the lowest, reflecting a 19% decrease. Similarly, in the $\langle 110 \rangle$ orientation, the peak velocity is 1.42×10^7 cm/s for the largest doping and 1.15×10^7 cm/s for the lowest, also a 19% reduction. The stronger quantum confinement in NW-FETs further amplifies the difference in average electron velocity between the $\langle 100 \rangle$ and $\langle 110 \rangle$ orientations. Across both devices, a higher doping enhances peak velocity. However, at the channel entrance (the source side) and exit (the drain side), lower doping exhibits higher velocity due to reduced scattering and improved electron mobility.

3.4. Interface roughness impact

Interface roughness refers to fluctuations, irregularities, or lattice mismatches at the semiconductor/dielectric interface, posing a key limitation in nanoscale devices. It significantly impacts ON current, subthreshold characteristics, and overall device performance by increasing carrier scattering and reducing mobility. Interface roughness scattering (IRS) is a critical

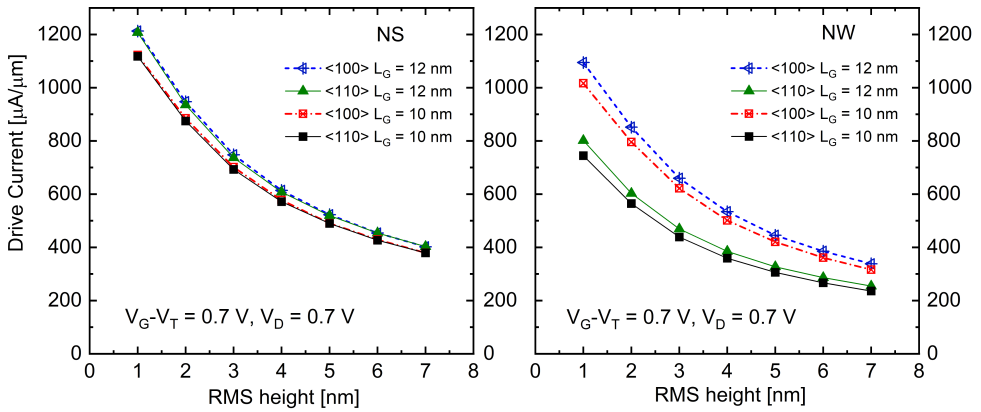

Fig. 11. The impact of RMS height (Δ_{RMS}) on the drive current (I_{DD}) for NS-FETs (left) and NW-FETs (right) with gate lengths of 12 nm and 10 nm, evaluated at an overdrive voltage of ($V_{\mathrm{G}} - V_{\mathrm{T}} = 0.7$ V) and a high drain bias of $V_{\mathrm{D}} = 0.7$ V.

performance-limiting factor in gate-all-around (GAA) devices, arising from atomic displacement at the silicon–dielectric interface, which alters the confining potential. In NS-FETs and NW-FETs, variations in channel geometry, such as; length, width, height, or gate length, affect the interface quality, typically altering the root-mean-square height (Δ_{RMS}). Our simulations employ Ando's model to account for electron scattering due to interface roughness. The Δ_{RMS} represents height fluctuations, and we explore Δ_{RMS} variation impact from 1.0 nm up to 7.0 nm in both NS- and NW-FETs, considering two gate lengths (12 nm and 10 nm) and two-channel orientations: $\langle 100 \rangle$ and $\langle 110 \rangle$, the correlation length (Λ_{cl}) kept fixed in all the simulations at 1.7 nm, as well as EOT (1.0 nm) and MDC (5×10^{19} cm^{-3}).

Figure 11 illustrates the impact of Δ_{RMS} on the drain current of NS-FETs (left) and NW-FETs (right) with gate lengths of 12 nm and 10 nm, respectively. An increase in the RMS height from 1.0 nm to 4.0 nm reduces the I_{DD} by 49.5% in the 12 nm L_G device, and 49% in the 10 nm L_G NS-FETs with $\langle 110 \rangle$ and $\langle 100 \rangle$ orientations. A further increase to 7.0 nm results in an additional 33.5% reduction in both cases. NW-FETs exhibit a similar trend. For the $\langle 110 \rangle$ channel, an increase from 1.0 nm to 4.0 nm in Δ_{RMS} reduces I_{DD} by 52% (12 nm L_G) and 51.5% (10 nm L_G), with an additional 34% reduction at 7.0 nm. For the $\langle 100 \rangle$ orientation, the corresponding reductions are 50.5% and 51% for 12 nm and 10 nm gate lengths, respectively, with further declines of 36.5% and 37% at 7.0 nm.

4. Conclusions

A state-of-the-art 3D FE MC device simulation toolbox, incorporating 2D SchEq quantum corrections, is employed to analyze the performance of NS-FETs and NW-FETs. Specifically, we study the impact of scaling gate length and oxide thickness, and changes in MDC and IR, on the performance of NS-FETs and NW-FETs, with a focus on optimizing the ON-current (I_{DD}). Reduction in the high-κ dielectric layer thickness improved I_{DD} in both devices, with a more pronounced effect in NS-FETs, particularly at $L_G = 10$ nm. Higher n-type doping concentrations enhanced I_{DD}, with NW-FETs benefiting more due to increased carrier injection from the

highly doped S/D regions. Gate length scaling to 10 nm resulted in a current reduction of approximately 9% in NS-FETs and 7% in NW-FETs. The threshold voltage (V_T) decreased from 0.29 V to 0.16 V as the S/D doping concentration increased. NW-FETs exhibited greater resilience to subthreshold degradation compared to NS-FETs. Device gate length, thickness, and width scaling were identified as critical factors for NS-FET design, directly influencing performance [6]. Interface roughness significantly impacted device performance. An increase in Δ_{RMS} from 1 nm to 4 nm reduces I_{DD} by approximately 49% and 52% in NS-FETs and NW-FETs, respectively. The impact is more pronounced in NW-FETs due to their higher surface-to-volume ratio.

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