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GaN Bootstrapped Logic Gates Analytical Modeling and Design Insights

Paul-Catalin MEDINCEANU[1] and Marius ENACHESCU[1, *]

[1]Dept. of Devices, Circuits and Architectures, National University of Science and Technology Politehnica Bucharest, Bucharest, Romania
Email: paul.medinceanu@stud.etti.upb.ro, m.enachescu@upb.ro*
* Corresponding author

Abstract. Following recent advancements, Gallium Nitride (GaN) technology continues to garner interest as a promising solution for future power electronics applications. Due to the variety of devices available in a monolithic GaN process, the development of digital circuits requires different topologies compared to CMOS technologies. This paper presents the analysis and design of logic gates from the bootstrapped family. Analytical equations for the static and dynamic parameters of an inverter are introduced. When compared to simulation results, these equations achieve a maximum error of 23.9% for static parameters and 33.3% for dynamic parameters. Additionally, different implementation details, such as developing other logic functions or enhancing the circuit behavior at system level, are proposed.

Key-words: Bootstrapped; DCFL; digital; GaN; gallium; gates; HEMT; inverter; logic; LSI; MSI; nitride; RTL; VLSI.

1. Introduction

In today's digitalized world, power conversion systems (PCS) are widely used in electronic applications such as portable devices, household appliances, and electric vehicles. These devices often rely on switching regulators (SRs) due to their high power density and conversion efficiency. Higher power density reduces the application's footprint, freeing up space for additional energy storage, while improved efficiency extends battery life and reduces heat dissipation [1].

SRs rely on semiconductor devices that act as switches to transfer and convert power from the source to the load. One such device is the Power MOS, which, in its advanced super junction MOS transistor design, supports breakdown voltages of up to 1kV while maintaining low conduction losses [2]. Despite these advancements, Si technology imposes a switching frequency

limit of 100kHz to 500kHz, which restricts the reduction of capacitor and inductor footprints and, consequently, the overall system power density [1].

To enhance the performance of PCSs, two alternative semiconductors have been adopted: Gallium Nitride (GaN) and Silicon Carbide (SiC) [3]. Meanwhile, other materials such as Diamond, Gallium Oxide (Ga_2O_3) and Aluminum Nitride (AlN) are being researched as possible solutions for future power devices [4]. GaN technology is particularly notable in low to mid-power applications due to its lower parasitic capacitance, reduced conduction resistance, and high breakdown voltage. These advantages, stemming from the High Electron Mobility Transistor (HEMT) structure and the material's physical properties, enable GaN devices to outperform their Si counterparts, offering a smaller footprint and the ability to switch at higher frequencies [5]. Due to the before mentioned performances, GaN devices have been used in commercial portable devices chargers [6].

Higher switching frequencies reduce the size of a SR's reactive components but also increase the impact of parasitic elements on system functionality. PCB traces, package leadframes, and bondwires create inductances along the signal path that controls the power switch (PS). These inductances, when interacting with other components, can form RLC circuits that may cause destructive gate overshoots or unintentionally turn the PS on or off [7]. One solution to this problem has been implemented at the package level by using bare dies [8] or by integrating the GaN PS with the CMOS gate driver using a multi-die approach [9]. To further reduce parasitic events, monolithic integration of power devices, control, and protection circuits in GaN technology has emerged. Due to the lack of an adequate p-type device in GaN [1], not all CMOS techniques can be used in designs. As a result, alternative logic families such as Resistor-Transistor Logic (RTL) [10], Direct-Coupled FET Logic (DCFL) [10], Pseudo-Complementary FET Logic (PCFL) [11], and Bootstrapped (BS) [12] have been used in digital circuits.

The analysis of the static parameters of the BS logic gates family was presented in [13], where design equations for device sizing, logic thresholds, and power consumption were developed, achieving predictions with a maximum error of 24% compared to simulations. This work extends the design framework by introducing equations for dynamic parameters such as rise time, fall time, and propagation delays. The proposed equations estimate these parameters with a maximum error of 33%. To gain insight into the stability and performance of the BS logic gates family within complex integrated circuits (ICs) across diverse operational conditions, we analyzed the characteristics of low-frequency switching stimuli.

The rest of the paper is organized as follows. Section 2. provides an overview of GaN technology and the most commonly adopted logic gate topologies. Section 3. presents the proposed design equations for the GaN BS family and discusses circuit design considerations. Section 4. compares the simulation and theoretical results for the analyzed GaN BS family.

Finally, the paper concludes in Section 5..

2. GaN Background

This section discusses the particularities of GaN technology, introduces the HEMT as the most commonly used device for monolithic integration, and details various logic gate families used in this process along with their potential applications.

2.1. GaN technology and devices

The main challenges and the principles of operation of the HEMT were discussed in this previous work [12]. This subsection builds upon and updates the previously published information. A significant obstacle that initially hindered the widespread adoption of GaN devices was the difficulty of producing large GaN wafers and the associated high costs, leading to the use of alternative substrates such as Si or SiC. Recently, a technological breakthrough enabled the production of 300mm wafers, a development that is expected to reduce GaN device prices in the long term [14].

As GaN technology evolves, the lateral HEMT remains the device of choice for monolithic integration in commercial processes. Nevertheless, researchers are also exploring vertical [15] and semi-vertical [16] structures, which offer higher breakdown voltages (exceeding 650V) and can be co-integrated with lateral devices. The high-voltage (HV) version of the HEMT is obtained by extending the drain and adding more field plates that deflect the high electric field away from the gate. The structures and cross-sectional views of the low-voltage (LV) and HV implementations are illustrated in Fig. 1 a) and Fig. 1 b), respectively, while the schematic symbols used in this work are shown in Fig. 1 c).

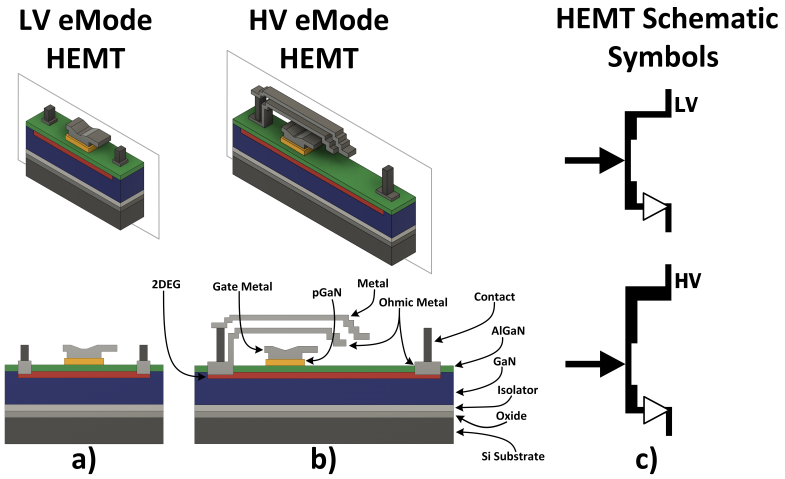

Fig. 1. HEMT Structures a) LV b) HV c) LV and HV symbols.

2.2. GaN logic gates

Due to the significant carrier mobility difference between n-type and p-type GaN devices, traditional CMOS logic gate topologies cannot be used in commercial technologies at this stage [17]. However, to overcome this, novel approaches that utilize the slower p-type HEMT to reduce power consumption have been proposed, as demonstrated in works like [18].

To address this technological limitation, alternative digital gate families have been used in GaN ICs, with their inverter schematics depicted in Fig. 2. These families are distinguished by the way the pull-up (PU) network is implemented. The most popular solutions include: using a resistor as a load (Fig. 2a), characteristic of the RTL family; using a depletion (d-mode) HEMT as a PU (Fig. 2b), as employed by the DCFL family; complementary control of the PU and

pull-down (PD) devices (Fig. 2c) to reduce static current, as seen in the PCFL family; and using a capacitor and diode to bootstrap the PU device, a technique used by the BS family (Fig. 2d).

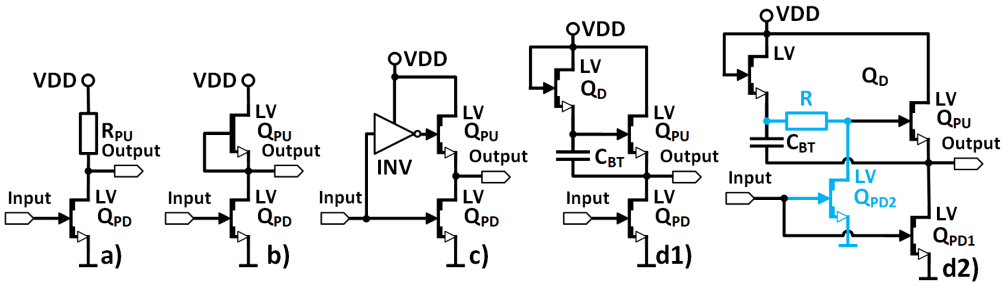

Fig. 2. GaN Inverters: a) RTL, b) DCFL, c) PCFL, and d1,d2) BS.

Digital circuits, particularly logic gates, require high-frequency operation with minimal delay and power consumption. As integration increases and functions become more complex, a compact footprint is also required. Additionally, high noise margins are critical to deliver the required performance and reliability in PCS, where high switched voltages and currents can introduce significant noise into the power supply.

The GaN ICs developed for PCS are mixed-signal designs, combining analog and digital circuits to perform various functions. The analog components handle tasks such as implementing overvoltage, overcurrent, or temperature protections, as well as generating and receiving clock signals [19]. Meanwhile, the digital components can be used as a gate driver for the PS [11], managing control loops to reduce cross-conduction current [20], generating different clock phases [19], enabling soft-start for SRs [21], and implementing state machines.

3. Designing with the GaN bootstrapped family

In this section, the BS family will be analyzed in detail from a design perspective, with the inverter (INV) topology from Fig. 2 d1) serving as the focus of the analysis. A comprehensive overview of the circuit will be presented, encompassing static, dynamic, and implementation considerations.

3.1. GaN bootstrapped inverter static parameters

The prior study [13] aimed to establish equations for device sizing, power consumption, and logic voltage levels. This paper incorporates these equations alongside newly developed equations for the dynamic parameters, resulting in a comprehensive set of design equations.

To size the bootstrap capacitor C_{BT} two approaches are presented: (1), which accounts for the allowable voltage ripple ΔV_{CBT}, the switching frequency f_{sw} and the leakage current I_{leak} of the PD device, and (2), derived from the relationship provided in [22].

Because the term $V_{DD} - V_{th} - V_D$, where V_{DD} is the supply voltage, V_{th} is the threshold of the transistor and V_D is the forward voltage of the diode connected device, appears frequently, it has been denoted with V_x in several of the following equations. (3) is intended to guide the selection of the aspect ratios of the PU and PD devices. By satisfying this equation, the switching point of the INV will be positioned at half of the supply voltage:

$$C_{BT} \geq \frac{I_{leak}}{\Delta V_{CBT} f_{sw}} \tag{1}$$

$$C_{BT} \geq (5 \div 10) \cdot C_{GS} \tag{2}$$

$$\frac{K_{PU}}{K_{PD}} = \frac{V_{DD} - 2V_{th}}{4(V_x)} \tag{3}$$

The equations that define the logic voltage levels are provided in: (4) for V_{IL}, (5) for V_{OL}, (6) for V_{IH}, and (7) for V_{OH}. These equations are subsequently used to calculate the circuit's noise margins: $NM_L = V_{IL} - V_{OL}$ and $NM_H = V_{OH} - V_{IH}$:

$$V_{IL} = \frac{K_{PU}(V_x)\sqrt{K_{PD}(K_{PD} + K_{PU})}}{K_{PD}(K_{PD} + K_{PU})} + V_{th} \tag{4}$$

$$V_{OL} = V_{DD} - V_{th} - \sqrt{(V_{DD} - V_{th})^2 - \frac{K_{PU}}{K_{PD}}(V_x)^2} \tag{5}$$

$$V_{IH} = \frac{2\sqrt{3}\sqrt{K_{PD}K_{PU}}(V_x)}{3K_{PD}} + V_{th} \tag{6}$$

$$V_{OH} = V_{DD} \tag{7}$$

The total power consumption (P_{total}) of the logic gate, calculated using (8) [13], is the sum of three components: dynamic power ($P_{dynamic}$), static power (P_{static}), and the power lost during the recharging of C_{BT} (P_{charge}):

$$P_{total} = \underbrace{C_{LOAD} \cdot V_{DD}^2 \cdot f_{sw}}_{P_{dynamic}} + \underbrace{\frac{1}{2} \cdot V_{DD} \cdot I_{PU}(sat)}_{P_{static}} + \underbrace{\frac{V_{DD} \cdot f_{sw} \cdot I_D}{2t_{charge}}}_{P_{charge}} \tag{8}$$

3.2. GaN bootstrapped inverter dynamic parameters

The timing diagrams presented in Fig. 3 illustrate the transfer characteristics of a BS inverter, emphasizing the specific time points at which the following parameters are measured: a) the propagation delays for transitions from high to low (t_{PHL}) and from low to high (t_{PLH}); and b) the rise time (t_R) and fall time (t_F). These dynamic parameters determine the maximum operational frequency of the BS inverter. Additionally, Fig. 3 depicts the operating regions of the devices and the load charging current ($I_{C_{LOAD}}$). Based on the reasoning presented in [23], $I_{C_{LOAD}}$ is treated as a linear function of time. This current varies according to the output voltage (V_{out}) and the operating regions of the PU and PD devices.

To illustrate the method for deriving timing equations, the deduction of (9), which represents the current during t_R, is explained. During the rise of V_{out} from 10% to 90%, the current $I_{C_{LOAD}}$ is determined using KCL, as the difference between the PU and PD currents. At 10%, the PU is in saturation, and the PD is in the linear region; at 90%, the PU is in the linear region, and the PD is in cutoff. Using these operating conditions and considering $I_{C_{LOAD}}$ a linear function, the right-hand side of (9) is expressed. Equating this to the capacitor's law, substituting dV_{out} with

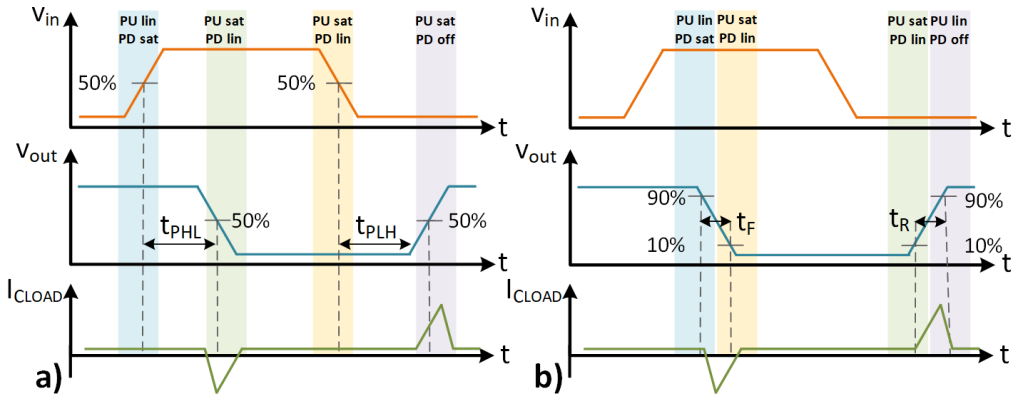

Fig. 3. Time diagrams: a)propagation times b)fall and rise times

$0.9V_{out} - 0.1V_{out}$, integrating over t_R, and solving for t_R yields (10). Similarly, the equations for t_{PLH}, t_{PHL}, and t_F are derived and provided in (12), (13), and (11), respectively:

$$C_{LOAD}\frac{dV_{out}}{dt} = \underbrace{I_{PU}(sat) - I_{PD}(lin) + \frac{[I_{PU}(lin) - (I_{PU}(sat) - I_{PD}(lin))]t}{t_R}}_{I_{C_{LOAD}}(t)} \tag{9}$$

$$t_R = \frac{1.6C_{LOAD}V_{DD}}{I_{PU}(sat) + I_{PU}(lin) - I_{PD}(lin)} \tag{10}$$

$$t_F = \frac{1.6C_{LOAD}V_{DD}}{I_{PD}(sat) + I_{PD}(lin) - I_{PU}(sat) - I_{PU}(lin)} \tag{11}$$

$$t_{PLH} = \frac{C_{LOAD}V_{DD}}{1.5I_{PU}(sat) - I_{PD}(lin)} \tag{12}$$

$$t_{PHL} = \frac{C_{LOAD}V_{DD}}{I_{PU}(sat) - 3I_{PU}(lin) + 2I_{PD}(sat)} \tag{13}$$

The minimum input stimuli frequency, f_{min}, required for C_{BT} to remain charged while the INV continuously outputs a high logic value is approximated by (14). This equation is derived by analyzing the time required for C_{BT} to discharge from its minimum charged voltage, $V_{CBT} - \frac{\Delta V_{CBT}}{2}$, due to the leakage current I_{leak}. The minimum voltage is considered because V_{CBT} decreases following the phase when the output was low, and C_{BT} was charged. The presence of V_{CBT} causes the source of Q_D to have a higher potential than its drain, resulting in a reverse leakage current flowing through it. At the output node, the leakage current of Q_{PD} is subtracted from this reverse leakage current, yielding $I_{leak} = I_{leakQ_D} - I_{leakQ_{PD}}$, which is used in this equation:

$$f_{min} \geq \frac{I_{leak}}{C_{BT}(V_{CBT} - \frac{\Delta V_{CBT}}{2})} \tag{14}$$

Simulations showed that after switching the INV and setting the input low, the output voltage drops below V_{OH} but remains within the sequential gate's NM_H. This reduced logic output level lowers the transconductance and, consequently, the current consumption of the next gate.

3.3. GaN bootstrapped logic family

Starting from the INV, the designs for other BS logic functions can be developed. The schematics for an N-input NAND gate and an N-input NOR gate are shown in Fig. 4 a) and b), respectively. The ratio from (3) can be applied to these gates by lumping the PD devices into a single transistor of equivalent size: for NANDs, the length is multiplied by the number of inputs, while for NORs, the width is multiplied.

The NAND implementation from Fig. 4 a) is based on this design [12], where additional bootstrap capacitors and diodes are connected to the nodes between the PD devices. This modification ensures proper operation, as without these additional components, the truth table of the NAND gate would only allow C_{BT} to charge when all inputs are high.

The operation of the PU network relies on a dynamic effect, requiring time for C_{BT} to charge and provide adequate overdrive voltage. Consequently, the initial transitions to a high level in a BS gate are slewed. To accelerate this phase, an additional PU device can be incorporated, analogous to the devices added in a NOR gate. This additional PU is controlled by a circuit similar to a power-on reset (POR) or undervoltage lockout (UVLO), which ensures that V_{out} is pulled low during startup and before normal operation begins.

Proposed variations aimed at reducing static current through the addition of a PD device and a resistor (marked in blue) are presented in [24], with a BS inverter depicted in Fig. 2 d2). However, this improvement leads to a slower rise time t_R.

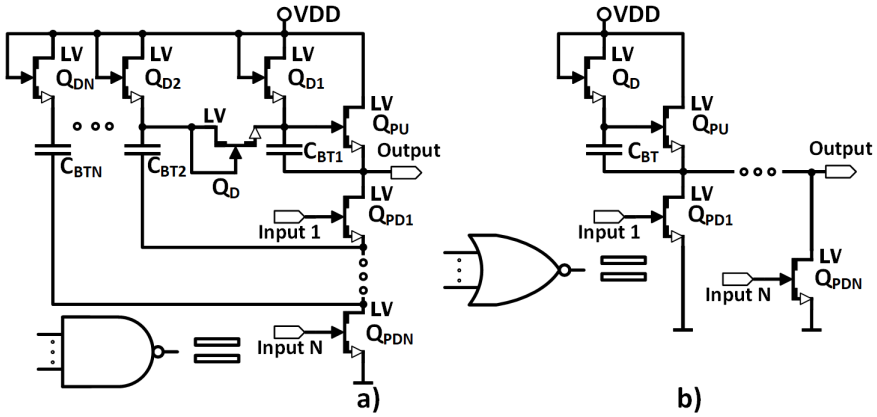

Fig. 4. GaN Logic Gates: a)NAND b)NOR.

4. Results

In this section, the developed INV circuits will be introduced, the simulation methodology is outlined, and the theoretical calculations and the simulation results for their parameters will be compared.

4.1. Analytic evaluation methodology

Using the equations derived in Section 3., inverters with different drive strengths and varying K_{PU}/K_{PD} ratios were developed using a 200V GaN process. The component sizing based on

these two characteristics is presented in Table 1. In this table, the columns represent the circuit characteristics, while the rows indicate the corresponding device sizes. The widths of the PU, PD, Q_D and the value of C_{BT} have been scaled proportionally to the drive strengths.

These circuits were evaluated for their static and dynamic parameters, as defined in Section 3., through SPICE simulations using the Cadence Virtuoso environment.

The method for measuring static parameters, accounting for the dynamic nature of the BS PU network, and power consumption has been detailed in [13]. Logic voltage levels were determined by sweeping the input voltage from ground (0 V) to the supply voltage (5 V). For the DC analysis, C_{BT} was assumed to be in a steady state with negligible ripple, and it was replaced with a DC voltage source set to V_{CBT}.

Dynamic performance was analyzed through transient simulations. Timing parameters were measured using a square wave input signal with a 50% duty cycle and a frequency of 10 MHz, while the load was set to approximate the equivalent of 4 INVs of the type being characterized. Parameters such as t_{PLH}, t_{PHL}, t_R, and t_F were determined by measuring the time intervals as illustrated in Fig. 3, while the f_{max} of each circuit was calculated as the mean of t_{PLH} and t_{PHL}. The ideal plot from Fig. 3 is reproduced through simulation in Fig. 5. Using the same setup, P_{total} was determined by measuring the average current drawn by the circuit over multiple clock periods after V_{CBT} had reached steady state and multiplying it by the supply voltage.

Table 1. Inverters sizing

K_{PU}/K_{PD}		1/2				1/3				1/4			
INV Drive / **Size (μm)**		*X1*	*X2*	*X4*	*X8*	*X1*	*X2*	*X4*	*X8*	*X1*	*X2*	*X4*	*X8*
Q_D	**W**	6	12	24	48	6	12	24	48	6	12	24	48
	L	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5
Q_{PU}	**W**	6	12	24	48	6	12	24	48	6	12	24	48
	L	7	7	7	7	10.5	10.5	10.5	10.5	14	14	14	14
Q_{PD}	**W**	6	12	24	48	6	12	24	48	6	12	24	48
	L	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5	3.5
C_{BT}	**C[fF]**	60	120	240	480	60	120	240	480	60	120	240	480

4.2. Analytic equations validation

The simulation results and theoretical values of the circuit parameters are summarized in Table 2. The columns categorize the values based on the drive strength of the INV, with the last column displaying the maximum error. Each drive strength category is further divided into two sub-columns: one for simulation values and one for theoretical values. The table is organized into three main rows, distinguishing between static and dynamic parameters for each K_{PU}/K_{PD} ratio. The error was calculated using (15).

It can be observed that the highest error for a static parameter appears for V_{OL} of the 1/4 INVs, with a value of 23.9%, while for the dynamic parameters, the highest error is exhibited by t_F of the 1/4 X8 INV with a value of 33.3%. Even though the percentage error of V_{OL} is considerable, the absolute difference of **88 mV** compared to **71 mV** is negligible. It can also be observed that the NM_H, NM_L, and $Power$ characteristics exhibit errors as low as 0.7% for the NM_H of the 1/3 INV, or even 0%, as is the case for the NM_L of the 1/2 INV. Regarding the dynamic

parameters, even though the errors reach 33.3%, as in the case of t_F of the 1/4 ratio X8 INV, the approximation method proposed in Section 3.2. provides values of the correct magnitude. This approach considers the device operation regions while avoiding complex mathematical functions that would otherwise complicate the design process.

$$Error = \frac{Simulation\,Value - Theoretical\,Value}{Simulation\,Value} \cdot 100\% \tag{15}$$

Table 2. Inverters simulation results

$\frac{K_{PU}}{K_{PD}}$	Parameter \ Name		*INVX1*		*INVX2*		*INVX4*		*INVX8*		Max Error
			Sim	Theo	Sim	Theo	Sim	Theo	Sim	Theo	
1/2	V_{OH}	**[V]**	5	5	5	5	5	5	5	5	0%
	V_{OL}	**[V]**	0.151	0.179	0.151	0.179	0.151	0.179	0.151	0.179	18.5%
	NM_H	**[V]**	1.211	1.227	1.211	1.227	1.211	1.227	1.211	1.227	1.3%
	NM_L	**[V]**	3.086	3.087	3.086	3.087	3.087	3.087	3.087	3.087	0%
	t_{PLH}	**[ns]**	5.077	4.92	3.911	3.36	3.389	3.256	3.131	3.167	14.1%
	t_{PHL}	**[ps]**	583	494	500	449	459	422	437	411	15.3%
	t_R	**[ns]**	12.03	9.22	8.132	7.095	6.469	6.285	5.782	5.894	23.4%
	t_F	**[ps]**	858	1045	755	998	704	921	677	899	32.8%
	f_{max}	**[MHz]**	353	369	453	525	519	543	560	559	15.8%
	$Power$	**[mW]**	0.301	0.301	0.588	0.583	1.158	1.156	2.295	2.295	0.9%
1/3	V_{OH}	**[V]**	5	5	5	5	5	5	5	5	0%
	V_{OL}	**[V]**	0.097	0.118	0.097	0.118	0.097	0.118	0.097	0.118	21.6%
	NM_H	**[V]**	1.422	1.413	1.422	1.413	1.422	1.413	1.423	1.413	0.7%
	NM_L	**[V]**	2.961	3	2.961	3	2.961	3	2.961	3	1.3%
	t_{PLH}	**[ns]**	7.263	5.355	5.711	5.064	5.017	4.893	4.665	4.798	26.5%
	t_{PHL}	**[ps]**	582	542	498	495	455	469	433	454	6.9%
	t_R	**[ns]**	16	12.06	10.96	9.445	9.041	9.116	8.213	7.771	24.6%
	t_F	**[ps]**	857	1011	750	941	696	899	668	882	32%
	f_{max}	**[MHz]**	255	339	322	360	366	373	392	381	33.03%
	$Power$	**[mW]**	0.211	0.204	0.41	0.401	0.806	0.799	1.594	1.588	3.3%
1/4	V_{OH}	**[V]**	5	5	5	5	5	5	5	5	0%
	V_{OL}	**[V]**	0.071	0.088	0.071	0.088	0.071	0.088	0.071	0.088	23.9%
	NM_H	**[V]**	1.554	1.524	1.554	1.524	1.554	1.524	1.555	1.524	2%
	NM_L	**[V]**	2.879	2.949	2.879	2.949	2.879	2.949	2.879	2.949	2.4%
	t_{PLH}	**[ns]**	9.44	7.39	7.597	6.877	6.717	6.61	6.25	6.484	21.7%
	t_{PHL}	**[ps]**	583	565	499	529	455	494	434	484	11.5%
	t_R	**[ns]**	18.88	15.68	13.82	13.17	11.68	12.06	10.78	11.55	16.9%
	t_F	**[ps]**	857	1000	747	936	689	898	661	881	33.3%
	f_{max}	**[MHz]**	200	251	247	270	279	282	299	287	26%
	$Power$	**[mW]**	0.166	0.156	0.32	0.311	0.626	0.616	1.237	1.225	6%

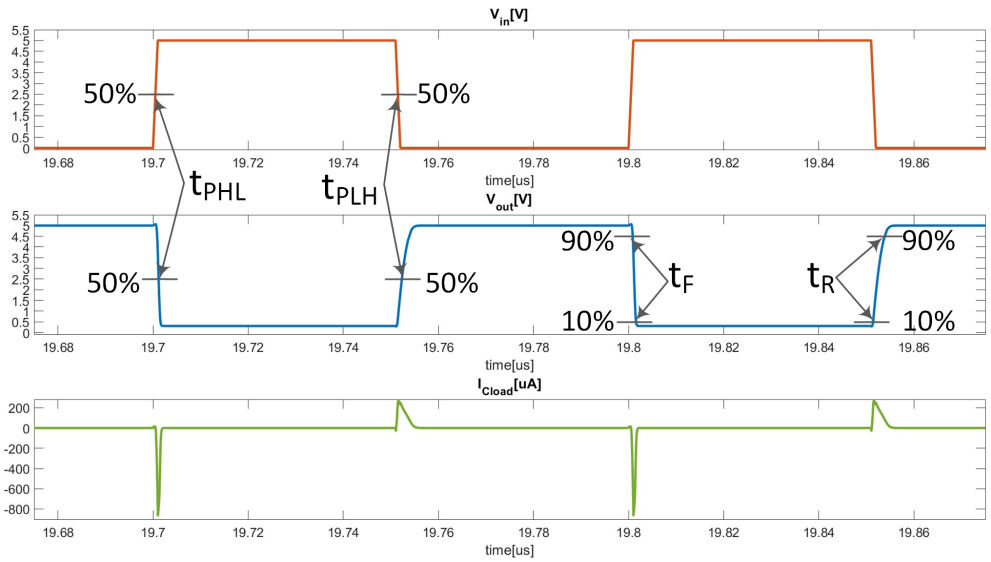

Fig. 5. GaN BS INV Transient Analysis.

5. Conclusions

In this paper, the analysis of the static parameters of the GaN BS logic gates family was extended to include dynamic parameters such as t_{PLH}, t_{PHL}, t_R, and t_F. The equations for the static parameters provided predictions with a maximum error of 23.9%, as observed for V_{OL}. The proposed approach for deriving GaN BS INV equations for dynamic parameters was validated by comparing the analytically calculated values with SPICE simulation results obtained using a Verilog-A-based device model.This method yielded a minimum error of 6.9% for t_{PHL} and a maximum error of 33% for t_F. Implementation practices, such as extending the INV design to NAND and NOR functions or incorporating further circuit enhancements, were proposed.

Acknowledgement.

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