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FinFET Model for Hand Calculation

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Abstract. A FinFET large signal device model for hand calculation DC analysis was developed using the Sah model as a reference and the available FinFET transistor models as fundation. First-order compact-model parameters were extracted and a new FinFET device-equation set is proposed in order to improve model accuracy compared to the Sah model (3% error vs ≈40% error). The proposed model provides valuable hints regarding circuit operation based on user definable FinFET parameters.

Key-words: Device modeling; FinFET; PDK; predictive technology model; Sah model.

1. Introduction

CMOS technology has been steadily scaled down to ultra-small sizes, resulting in significant challenges such as short channel effects, high power densities, and increased leakage currents. As conventional MOSFETs struggle at technology nodes below 32nm, the focus has shifted to alternative approaches at 22nm and 14nm, where FinFETs have emerged as the solution and had become the *de facto* standard for the to date advanced process nodes. FinFETs use a thin silicon "fin" as the channel region, enclosed by an wrap-around gate structure that provides enhanced electrostatic control, thereby reducing leakage currents and alleviating short channel effects [1].

Since FinFET is a relatively recent technology and the primary goal is fabrication process improvement, information disclosed by manufactures is rather scarce. Therefore, the foundries provides very limited access to simulation models and their parameters. After extracting parameters for the classical Sah-Model, poor model accuracy was observed and a different model should be used. The main objective was to get a FinFET device model appropriate for hand calculation. Systematic analysis of the specific literature did not indicate such a model. The foundation was build on the Cadence Generic 0.8V/1.8V PDK (cds_ff_mpt)®, GPDK, the FinFET Predictive Technology Model, PTM, from the Department of Electrical and Computer Engineering at the University of Minnesota and the Synopsys SAED_PDK14_FinFET®, SAED14.

This paper reveals in Section 2 the aim of the research. A short description of each FinFET device type is presented in Section 3 followed by the FinFET Sah-Model paramater extraction procedure in Section 4. The proposed FinFET device model is developed in Section 5 and validated in Section 6. Conclusions and further improvements are formulated in Section 7.

2. Scope of the Research

In every circuit design project (analog or digital), the path from general concept to final product should follows a rigorous algorithm:

1. **Choose device technology:** The designer must knows its devices, how to control and what she/he can do with them;
2. **Design the circuit(s) "by hand":** What fundamental structures are needed, advantages vs disadvantages, proper sizing and dimensioning, actual design specs etc;
3. **Simulate the designed circuit(s):** The simulations must validate the "by hand" design;
4. **Final product implementation:** Re-simulation including parasitics must validate again both simulations and the "by hand" design.

For planar MOS device the above algorithm is facilitated by:

1. Clear and complete knowledge of the device types and their specific parameters;
2. Clear and complete knowledge regarding how to control & what can be done with it;
3. Clear implementation of the project ("by hand" design, simulations, final product).

For FinFET device the above algorithm faces some important challenges:

1. Incomplete/ hard to find knowledge about device types and their specific parameters;
2. Incomplete/ hard to find knowledge regarding how to control & what can be done with it.

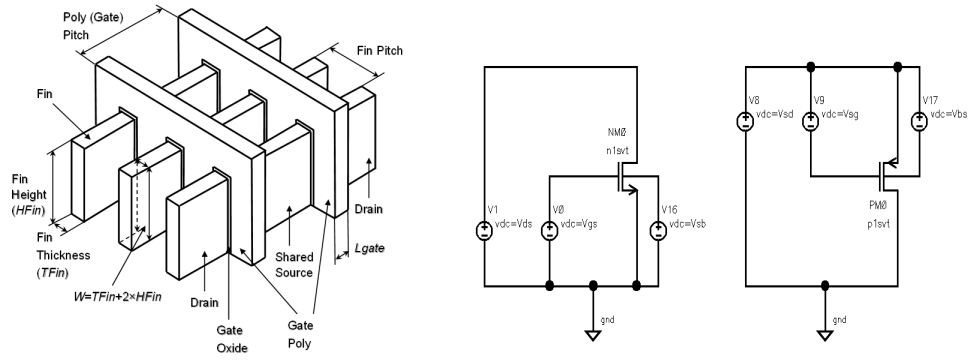
To put it into perspective, the existing models in the specialized literature are too complex to be handled analytically (suitable only for simulators). Moreover, they focus on a particular physical phenomena or operating mode [2], [3]. After a meticulous investigation, a simplified FinFET transistor model, adequate for hand calculation, was not identified. The Sah model gives unacceptable results. In the light of these, the first 2 step of the algorithm presented above are missing for the FinFET technology and a simplified hand calculation model is necessary. Please note, that he term "hand calculation" refer to the manual design of a FinFET circuit, followed by the simulation validation (and not jumping directly to the simulation as it is the case today).

3. FinFET Transistors Models

Before presenting the FinFET device modeling process, one must first get acquainted with the devices (types, specific parameters, parameter values, which parameters are transparent to the designer and which are not, how they influence the behavior of the device). The characterization testbench is shown in Fig. 1b and was used to perform the parameter extraction process for GPDK, PTM and SAED14 FinFET transistors. The methodology used to develop the three models is not disclosed by the respective owners. The simulations were carried out using Cadence Spectre®. Fig. 1a presents a FinFET structure with the following parameters:

- **Fin Pitch** (FP) – Distance between 2 fins;

- **Fin Height** (HFin) – The height of a single fin;
- **Fin Thickness** (TFin) – The thickness of a single fin;
- **Number of Fins per Finger** (NFins);
- **Poly Pitch** (PP) – Distance between 2 poly gates;
- **Gate Length** (Lgate) – Only two or three gate lengths are permitted usually [4];
- **Transistor Width** (W) = TFin + 2·HFin;
- **Number of Fingers** (F) – Number of poly gate fingers used in layout;
- **Multiplier** (M) – Number of parallel MOS devices.



(a) Structure and parameters (b) Device characterization testbench

Fig. 1. FinFET device [5].

3.1. Cadence's Generic 0.8V/1.8V PDK®

In the FinFET transistor model set provided by GPDK, one can distinguish 3 MOS transistor types: **HVt** (**H**igh V_T), **SVt** (**S**tandard V_T) and **LVt** (**L**ow V_T). As specific parameters (see Fig. 1a) there are FP, NFins, PP, Lgate, F & M but only NFins, PP (with only 5 possible values), Lgate (with only 5 possible values) while F & M parameters take integer user definable values [6]. The device name convention used for FinFET transistors from GPDK is presented in Table 1.

Table 1. Device name convention for Cadence's Generic 0.8V/1.8V PDK®

Device name	Device name sections		
	Length	Channel type	Device type
XXnm_YCh_ZV$_T$	XX[nm]	Y = **N** → **N**MOS Transistor Y = **P** → **P**MOS Transistor	Z = **L** → **L**ow V_T MOS Transistor Z = **S** → **S**tandard V_T MOS Transistor Z = **H** → **H**igh V_T MOS Transistor
e.g. 20nm_NCh_HVt	20nm	NMOS	High V_T
e.g. 24nm_PCh_LVt	24nm	PMOS	Low V_T

3.2. Predictive Technology Model (PTM)

In deep-submicron technologies, physical effects such as process variations, mobility degradation, and power consumption require advanced circuit design techniques. Predictive Technology Models (PTMs) provide accurate and scalable models for current and future technology nodes, enabling reliable analog circuit design for emerging transistor architectures, including FinFETs and Gate-All-Around (GAA) devices, at technology nodes of 7 nm and below [7].

For the 24nm to 11nm FinFET transistor models provided by PTM, one can distinguish 2 MOS transistor types: **HP** (**H**igh **p**ower) and **LSTP** (**L**ow & **St**andard **p**ower). As parameters there are (see Fig. 1a) HFin, TFin (with specific values for each device), Lgate (with only 5 possible values), NFins and M (that may take any integer user define value) [8]. Table 2 present the device name convention used for FinFET transistors from PTM.

Table 2. Device name convention for Predictive Technology Model (PTM)

Device name	Device name sections		
	Length	Channel type	Device type
XXnm_YCh_ZPow	XX[nm]	Y = **N** → **N**MOS Transistor Y = **P** → **P**MOS Transistor	Z = **LST** → **L**ow & **St**andard power MOS Transistor Z = **H** → **H**igh power MOS Transistor
e.g. 18nm_NCh_LSTP	18nm	NMOS	Low & Standard power
e.g. 18nm_PCh_HP	18nm	PMOS	High power

3.3. Synopsys SAED_PDK14_FinFET®

In the FinFET transistor set provided by SAED_PDK14_FinFET® (**S**ynopsys **A**rmenia **E**ducational **D**epartment, **P**rocess **D**esign **K**it, 14nm FinFET), one can distinguish 3 MOS transistor types: **HVt** (**H**igh $\boldsymbol{V_T}$), **LVt** (**L**ow $\boldsymbol{V_T}$) and **SLVt** (**S**uper**l**ow $\boldsymbol{V_T}$). As specific parameters (see Fig. 1a) there are FP (32nm only), NFins, Lgate (14nm only), F & M but only NFins, F & M parameters take integer user definable values [9]. Table 3 present the device name convention used for this FinFET transistors type.

Table 3. Device name convention for Synopsys SAED_PDK14_FinFET®

Device name	Device name sections		
	Length	Channel type	Device type
XXnm_YCh_ZV$_{\mathrm{T}}$	XX[nm]	Y = **N** → **N**MOS Transistor Y = **P** → **P**MOS Transistor	Z = **SL** → **S**uper**l**ow V_T MOS Transistor Z = **L** → **L**ow V_T MOS Transistor Z = **H** → **H**igh V_T MOS Transistor
e.g. 14nm_NCh_HVt	14nm	NMOS	High V_T
e.g. 14nm_PCh_LVt	14nm	PMOS	Low V_T

4. FinFET Sah-Model Parameter Extraction

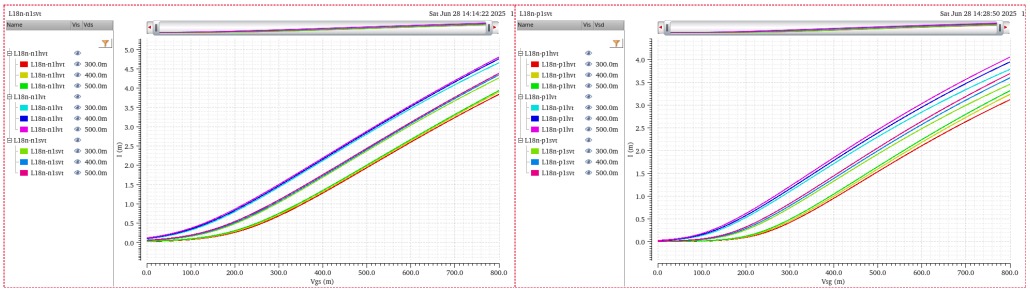
Before transistor models can be used for hand calculation, model parameters that capture device specific characteristics must be determined. Because these parameters are not provided by the wafer manufacturer, the devices must be characterized by simulation in order to obtain the data required for design. From the fundamental quadratic Sah model of the planar MOS transistor [10], the graphical and numerical methods described in [11] were applied in order to extract the model parameters [5]. This paper is an extension of the previous work reported in [5]. The presented FinFET parameter extraction analysis, together with the elements introduced in the following sections, serves as the basis for the proposed FinFET model.

4.1. Extraction of the zero biased bulk threshold voltage, V_{T0}, and saturation conduction parameter, K

In order to extract V_{T0} and K, the quadratic equation that describes a MOS transistor operating in strong inversion and saturation was used. It was evaluated $\sqrt{I_D}(V_{GS})$, that, in the saturation region, should exhibit a linear behavior. It was computed m_{ij} and V_{T0_ij} (there were

chosen n measuring points and then used consecutive pair of points "i" and "j"). By applying linear regression, the slope m is obtained (and similarly V_{T0}). Special attention must be paid, since second-order effects such as weak inversion currents near $V_{GS} = V_{T0}$ and mobility degradation at high V_{GS} values may distort the best-fit line.

Therefore, data points that significantly deviate from the model should be excluded [11]. For the extraction of V_{T0} & K by means of linear regression, the $\sqrt{I_D}(V_{GS})$ characteristics shown in Fig. 2a were used for NMOS FinFET transistors, while the characteristics in Fig. 2b were used for PMOS FinFET transistors.



(a) for NMOS FinFET transistors (b) for PMOS FinFET transistors

Fig. 2. $\sqrt{I_D}(V_{GS})$ characteristics [5].

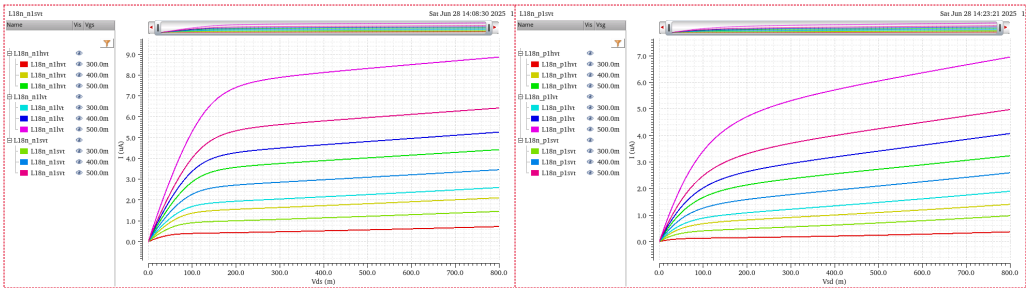
4.2. Extraction of the channel length modulation parameter, λ

For the extraction of λ, the slope of $I_D(V_{DS})$ in the saturation region was measured. The parameter λ can then be calculated as the ratio between the slope m and the y intercept, I_{D0}. Linear regression was applied to determine m and I_{D0}. For the extraction of λ and I_{D0}, the $I_D(V_{DS})$ characteristics shown in Fig. 3a were used for NMOS FinFET transistors, while those in Fig. 3b were used for PMOS FinFET transistors [11].

4.3. Extraction of substrate factor, γ

To extract γ, the quadratic equation describing a MOS transistor in strong inversion and saturation was used again. It was determined V_{T0} from $\sqrt{I_D}(V_{GS})$. Next, $\sqrt{I_D}(V_{GS})$ was plotted for different V_{SB} values. For each V_{SB}, the corresponding V_T was obtained. The $V_T(V_{SB})$ dependence was then represented and the slope m measured between two points "i" and "j" on this line provides the parameter γ [11]. To reclaim the gate control over the channel, the innovative idea that led to the creation of FinFET was to place the channel vertically and wrap the gate around it on lateral and top sides.

The only side that the body-effect can modulate the channel is from below, where there is no gate. For these reason, the body-effect is significantly reduced for FinFET devices. As a consequence, γ parameter extraction procedure was performed only for GPDK FinFET transistors since PTM and SAED14 FinFET transistors models choose to not include the substrate effect. In contrast, the same parameter extraction procedure of V_{T0}, K and λ was used for GPDK, PTM and SAED14 FinFET transistors.



(a) for NMOS FinFET transistors (b) for PMOS FinFET transistors

Fig. 3. $I_D(V_{DS})$ characteristics [5].

4.4. Integer User Defined Parameter Analysis

The characterization results for this type of parameters are presented in Table 4 for GPDK, PTM and SAED14 FinFET transistors. The effect of the number of fins (NFin) on the device characteristics/ parameters was analyzed and the following conclusions were reported:

- NFin **does not affect** V_{T0}, λ and γ;
- NFin **affect** K as a multiplication constant;
- NFin and M **have the same effect** (from electrical point of view).

Table 4. Example of parameter extraction results for several devices

Device type (GPDK)	Device parameters			
	V_{T0}[mV]	$K[\mu A/V^2]$	$\lambda[V^{-1}]$	γ
18nm_NCh_HVt	190.73	84.13	0.66	0.13
18nm_NCh_LVt	54.57	84.76	0.42	0.16
18nm_NCh_SVt	126.50	86.06	0.49	0.14

Device type (GPDK)	Device parameters			
	V_{T0}[mV]	$K[\mu A/V^2]$	$\lambda[V^{-1}]$	γ
18nm_PCh_HVt	204.78	62.73	1.48	0.14
18nm_PCh_LVt	44.57	58.49	1.12	0.18
18nm_PCh_SVt	126.23	60.99	1.31	0.16

Device type (PTM)	Device parameters		
	V_{T0}[mV]	$K[\mu A/V^2]$	$\lambda[V^{-1}]$
18nm_NCh_LSTP	365.39	616.65	4.76
18nm_NCh_HP	123.49	434.66	0.96

Device type (PTM)	Device parameters		
	V_{T0}[mV]	$K[\mu A/V^2]$	$\lambda[V^{-1}]$
18nm_PCh_LSTP	366.58	552.11	8.54
18nm_PCh_HP	135.07	407.15	1.34

Device type (SAED14)	Device parameters		
	V_{T0}[mV]	$K[\mu A/V^2]$	$\lambda[V^{-1}]$
14nm_NCh_HVt	351.37	1250.67	0.89
14nm_NCh_LVt	274.21	1188.72	0.83

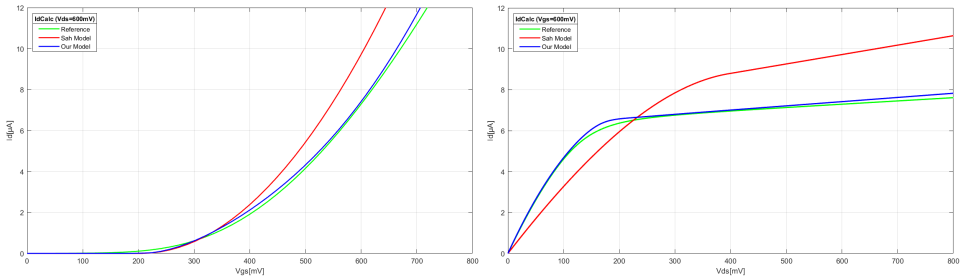
Device type (SAED14)	Device parameters		
	V_{T0}[mV]	$K[\mu A/V^2]$	$\lambda[V^{-1}]$
14nm_PCh_HVt	297.62	798.13	0.91
14nm_PCh_LVt	227.37	906.36	1.02

Different NFin and M will lead to different active area and power dissipation density: increasing the number of fins allows for higher current within a smaller area compared to increasing the multiplicity. However, too many fins may lead to excessive power dissipation density, thus adjusting the multiplicity may provide a solution by spreading power over larger area. Additionally, device matching may differ when comparing transistors with the same total width but different combinations of NFin and M. Device matching issue will be addressed in future work.

5. Proposed Model for Hand Calculations

In order to validate the extracted parameters, the devices characteristics based on GPDK/ PTM/ SAED14 models were compared with the characteristics provided by the Sah model. The results are presented in Fig. 4a for the $I_D(V_{GS})$ characteristics and in Fig. 4b for the $I_D(V_{DS})$ characteristics. It is easy to observe that the Sah model (red) gives highly inaccurate device

characteristics: the transition between linear and saturation region happens earlier than predicted by the Sah model (i.e. different equation for V_{DS_Sat}), linear region is much smaller (i.e. different equation for the linear region), saturation region is much bigger (i.e. different equation for the saturation region) and, finally, the slope of the characteristic both in linear and saturation region is different (i.e. different behavior of the λ).



(a) $I_D(V_{GS})$ characteristics (b) $I_D(V_{DS})$ characteristics

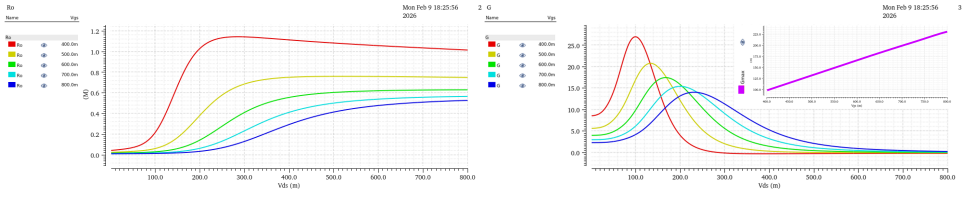
Fig. 4. Comparison between original devices characteristics (green), characteristics provided by the Sah model (red) and our model (blue).

The evolution of the proposed model (blue in Fig. 4) is presented further. It is an empirical model and it can be used only for single-gate transistors (the majority of the planar MOS transistor model also does not include geometry dependent effects specific to double-gate or triple-gate structure). The Sah model was used as a starting point. The mismatches were treated one by one, solutions for each one of them were established and the correction to the Sah model were made:

1. $\boldsymbol{V_{DS\_Sat}}$ **issue**: After researching this matter in the specialized literature, the usage of the G function approach proposed in [12] was decided, as it relies on the general I–V characteristics and does not depend on any particular device model or type. The G function is defined as follows (r_o is the output resistance of the device):

$$G = \frac{1}{r_o}\frac{\partial r_o}{\partial V_{DS}}. \tag{1}$$

As illustrated in Fig. 5b, the G function value increases in the linear region until it reaches a maximum, and then decreases in the saturation region (i.e. the slope of the G function, $\frac{\partial r_o}{\partial V_{DS}}$, is positive in the linear region and becomes negative in the saturation region). Therefore, the value of V_{DS_Sat} can be determined from the peak of the G function, that serves as the transition point between the linear and saturation regions [13].



(a) Output resistance, r_o (b) G function

Fig. 5. Output resistance, r_o, and G function of a FinFET device.

By extracting the peaks of the G function with respect of V_{GS}, one can observe a linear dependence between them (violet graph from Fig. 5b right corner). This means that V_{DS_Sat}

can be written as function of V_{GS} as follows (for Sah model see [10]):

$$V_{DS\_Sat}(V_{GS}) = x_0 + x_1 \cdot V_{GS}. \quad (2)$$

where x_0 and x_1 are real constant empirically determined. In Fig. 5a it is worth to observe the behavior of the output resistance r_o that increases in the linear region, reaches a maximum and then decreases in saturation. This implies that saturation gain cannot be assumed to be constant as is the case in planar devices.

2. **Linear region issue**: In the linear region the constants K and those multiplying V_{T0} and V_{DS} in the Sah model prove to be inappropriate. By extracting these constants with respect to V_{GS}, the following conclusions can be drawn: the K constant in linear region is 4 times bigger than in saturation region and the factors multiplying V_{T0} and V_{DS} are no longer constant and depend on V_{GS}. The proposed form for the current equation in linear region is (for Sah model see [10]):

$$I_D(V_{GS}) = 4 \cdot K \cdot V_{DS} \cdot (V_{GS} - f_{V_{T0}}(V_{GS}) \cdot V_{T0} - f_{V_{DS}}(V_{GS}) \cdot V_{DS}) \cdot (1 + \lambda(V_{GS}) \cdot V_{DS}). \quad (3)$$

where $f_{V_{T0}}(V_{GS})$ is the function that gives us the factor that multiplies V_{T0}, that varies with respect to V_{GS} and has the following form:

$$f_{V_{T0}}(V_{GS}) = y_0 + y_1 \cdot V_{GS}. \quad (4)$$

where y_0 and y_1 are empirically determined real constants. $f_{V_{DS}}(V_{GS})$ is the function that provides the V_{DS} multiplying factor that also varies with respect to V_{GS} like:

$$f_{V_{DS}}(V_{GS}) = z_0 + z_1 \cdot V_{GS} + z_2 \cdot V_{GS}^2. \quad (5)$$

where z_0, z_1 and z_2 are empirically determined real constants.
$\lambda(V_{GS})$ dependence will be discussed in Section 4.

3. **Saturation region issue**: The values for K division factor and V_{T0} and V_{GS} multiplying factors depend on V_{GS}. By extracting these factors with respect of V_{GS}, one may came to the following conclusions: the K division factor is dependent on V_{GS} and, V_{T0} and V_{GS}, multiplying factors are independent on V_{GS}. The proposed equation for the current in saturation region is (for Sah model see [10]):

$$I_D(V_{GS}) = \frac{K}{\alpha}(V_{GS} - V_{T0})^2 \cdot (1 + \lambda(V_{GS}) \cdot V_{DS}) \quad (6)$$

where α is a empirically determined real constant.

4. **λ (channel-length modulation) behavior issue**: The λ parameter exhibits a V_{GS} dependence. The proposed $\lambda(V_{GS})$ function is presented bellow:

$$\lambda(V_{GS}) = \beta_0 + \beta_1 \cdot V_{GS} + \beta_2 \cdot V_{GS}^2 + \beta_3 \cdot V_{GS}^3. \quad (7)$$

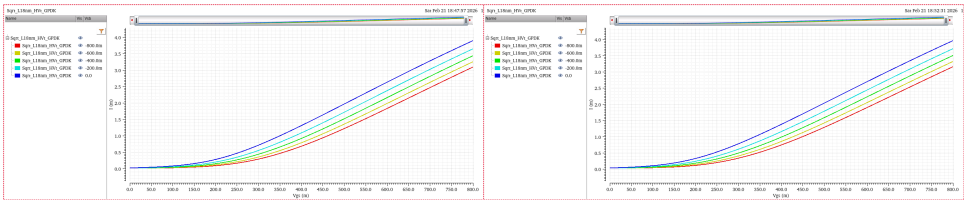
where β_0, β_1, β_2 and β_3 are empirically determined real constants.

Incorporated physical effects
The following FinFET specific effects were added: V_{DS_Sat} dependence on the $\max(G)$ function, NFin acting as a multiplication factor, operating mode dependent conduction parameter ($4K$ in the linear region and K in saturation), the influence of $f_{V_{T0}}(V_{GS})$ and $f_{V_{DS}}(V_{GS})$ in the linear region, α dependent saturation behavior and $\lambda(V_{GS})$ dependence.

Quantization effect
Following the results obtained in Section 4.4, the quantization effect does not affect V_{T0},

λ and γ, it affect only K as a simple multiplication constant. To take into account this effect, one must multiply the current equations for each region with the number of fins, NFin.

Substrate effect behavior (GPDK only)
In Fig. 6, the $\sqrt{I_D}(V_{GS})$ characteristics were plotted for different V_{DS} and V_{BS}. After investigating the behavior of the substrate effect in different scenarios, it can be concluded that γ is independent with respect to V_{DS} and the classical $V_T(V_{BS})$ equation is still valid.



(a) For different V_{BS} and V_{DS} = 400mV (b) For different V_{BS} and V_{DS} = 600mV

Fig. 6. $\sqrt{I_D}(V_{GS})$ characteristics.

Table 5. Summary of the proposed model

Model parameters review	Model limitation
The proposed model uses the K, V_{T0} and γ classical parameters, introduces a new parameter α and replaces the other parameters with values computed based on V_{GS} using different empirically constants as follows: • $V_{DS\_Sat}(V_{GS}) \leftarrow x_0$ and x_1; • $f_{V_{T0}}(V_{GS}) \leftarrow y_0$ and y_1; • $f_{V_{DS}}(V_{GS}) \leftarrow z_0$, z_1 and z_2; • $\lambda(V_{GS}) \leftarrow \beta_0$, β_1, β_2 and β_3; Equation complexity greatly increased!	Designed only for DC analysis. Discontinuous transition between linear and saturation region. Similar to the Sah model, the proposed model does not include: • Short-channel effects; • Mobility degradation effect; • Velocity saturation effect; • Geometry specific effects; • TFin and HFin effects; • DIBL effect.

Parameters extraction procedure	
The proposed model is general for all FinFET models, but the empirical real constants must be fitted separately to each model library. • α is obtained empirically. • Compute $max(G)$ @ $V_{GS} \in$ [400,800]mV, 100 mV steps $\rightarrow$ apply linear regression on data set $\rightarrow$ x_0 - x_1 are found. For each $\sqrt{I_D}(V_{GS})$ @ $V_{DS} \in$ [400,800]mV, 100 mV steps: • Apply Section 4.1 procedure $\rightarrow$ V_{T0} and K data set is obtained; For each $I_D(V_{DS})$ @ $V_{GS} \in$ [400,800]mV, 100 mV steps:	• Apply Section 4.2 procedure $\rightarrow$ λ data set is obtained $\rightarrow$ apply cubic regression $\rightarrow$ β_0 – β_3 are obtained; • Apply quadratic regression in the linear region $\rightarrow$ normalize by $4K$ the regression coefficient $\rightarrow$ the quadratic term constant is the V_{DS} multiplying factor $\rightarrow$ quadratic regression is used on the V_{DS} multiplying factor data set $\rightarrow$ z_0 - z_2 are found; • $V_{GS} - V_{T0}$ divided by the linear term constant obtained above is the V_{T0} multiplying factor $\rightarrow$ quadratic regression is used on the V_{T0} multiplying factor data set $\rightarrow$ y_0 - y_1 are found;

6. Model Validation

Tables 6–8 summarize the extracted FinFET model parameters for the GPDK, PTM, and SAED14 technologies, respectively. It should be noted that all empirical constants depend on

both the gate length, Lgate, and the device type. Figures 7–9 compare the original transistor characteristics (*/NM1/D* or */PM0/S* for GPDK and */M0/D* or */M0/S* for PTM and SAED14) with those obtained using the proposed model (*IdCalc*) for each technology.

Overall, the proposed model accurately reproduces the device characteristics for both NMOS and PMOS FinFETs over the range $V_{GS} \in [V_T, 600]$mV, $\forall V_{DS}$ (with $V_T \in [100, 350]$mV). At V_{GS} = 700mV, the accuracy deteriorates and barely work for $V_{DS} \in [300, 500]$mV, while at V_{GS} = 800mV the model exhibits significant deviations because it does not include the mobility degradation effects. Furthermore, the transition between the linear and saturation regions is not perfectly smooth and can be improved using a sigmoid function (optional for hand calculation).

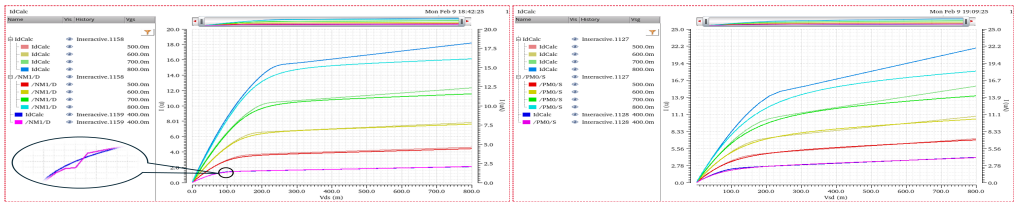
Table 6. FinFET modelling results for Cadence Generic 0.8V/1.8V PDK®

Device type	Device model parameters		
	V_{T0}[mV]	V_{DS_Sat}[mV]	$K[\mu A/V^2]$
18nm_NCh_HVt	190.73	$V_{DS\_sat} = \frac{V_{GS}}{3}$	84.13

Device type	Device parameters		
	V_{T0}[mV]	V_{SD_Sat}[mV]	$K[\mu A/V^2]$
18nm_PCh_LVt	44.57	$V_{SD\_sat} = \frac{V_{SG}}{3}$	58.49

Device type	Linear region	
	The coefficient function of V_{T0}, $f_{V_{T0}}(V_{GS})$	The coefficient function of V_{DS}, $f_{V_{DS}}(V_{GS})$
18nm_NCh_HVt	$f_{V_{T0}}(V_{GS}) = 2.10\|2.18 \cdot V_{GS} + 0.81$	$f_{V_{DS}}(V_{GS}) = -0.80 \cdot V_{GS}^2 + 1.50 \cdot V_{GS} - 0.20$
18nm_PCh_LVt	$f_{V_{T0}}(V_{SG}) = 5.10\|5.20 \cdot V_{SG} + 1.54$	$f_{V_{SD}}(V_{SG}) = -0.86 \cdot V_{SG}^2 + 1.51 \cdot V_{SG} + 0.048$

Device type	Saturation region equation	Channel length modulation effect, $\lambda(V_{GS})$
18nm_NCh_HVt	$\frac{K}{2.50\|2.25}(V_{GS} - V_t)^2 \cdot (1 + \lambda(V_{GS}) \cdot V_{DS})$	$\lambda(V_{GS}) = -11.30 \cdot V_{GS}^3 + 24.98 \cdot V_{GS}^2 - 18.03 \cdot V_{GS} + 4.60$
18nm_PCh_LVt	$\frac{K}{3.07\|2.83}(V_{SG} - V_t)^2 \cdot (1 + \lambda(V_{SG}) \cdot V_{SD})$	$\lambda(V_{SG}) = -8.84 \cdot V_{SG}^3 + 19.87 \cdot V_{SG}^2 - 14.06 \cdot V_{SG} + 4.13$



(a) Modelling results for 18nm_NCh_HVt (b) Modelling results for 18nm_PCh_LVt

Fig. 7. Original devices characteristics (/NM1/D or /PM0/S) vs Our model (IdCalc) for GPDK.

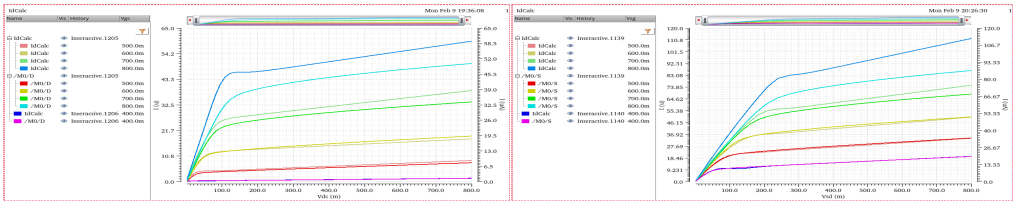
Table 7. FinFET modelling results for Predictive Technology Model (PTM)

Device type	Device model parameters		
	V_{T0}[mV]	V_{DS_Sat}[mV]	$K[\mu A/V^2]$
18nm_NCh_LSTP	365.39	$V_{DS\_sat} = \frac{V_{GS}}{4}$	616.65

Device type	Device parameters		
	V_{T0}[mV]	V_{SD_Sat}[mV]	$K[\mu A/V^2]$
18nm_PCh_HP	135.07	$V_{SD\_sat} = \frac{V_{SG}}{3}$	407.15

Device type	Linear region	
	The coefficient function of V_{T0}, $f_{V_{T0}}(V_{GS})$	The coefficient function of V_{DS}, $f_{V_{DS}}(V_{GS})$
18nm_NCh_LSTP	$f_{V_{T0}}(V_{GS}) = 1.82\|1.71 \cdot V_{GS} + 0.33$	$f_{V_{DS}}(V_{GS}) = -11.08 \cdot V_{GS}^2 + 13.28 \cdot V_{GS} - 3.34$
18nm_PCh_HP	$f_{V_{T0}}(V_{SG}) = 6.15\|5.85 \cdot V_{SG} - 0.55$	$f_{V_{SD}}(V_{SG}) = 2.07 \cdot V_{SG}^2 - 3.95 \cdot V_{SG} + 2.12$

Device type	Saturation region equation	Channel length modulation effect, $\lambda(V_{GS})$
18nm_NCh_LSTP	$\frac{K}{2.50\|2.77}(V_{GS} - V_t)^2 \cdot (1 + \lambda(V_{GS}) \cdot V_{DS})$	$\lambda(V_{GS}) = -211.48 \cdot V_{GS}^3 + 431.40 \cdot V_{GS}^2 - 291.37 \cdot V_{GS} + 65.79$
18nm_PCh_HP	$\frac{K}{3.00\|2.73}(V_{SG} - V_t)^2 \cdot (1 + \lambda(V_{SG}) \cdot V_{SD})$	$\lambda(V_{SG}) = -13.86 \cdot V_{SG}^3 + 35.03 \cdot V_{SG}^2 - 27.70 \cdot V_{SG} + 7.70$



(a) Modelling results for 18nm_NCh_LSTP (b) Modelling results for 18nm_PCh_HP

Fig. 8. Original devices characteristics (/M0/D or /M0/S) vs Our model (IdCalc) for PTM.

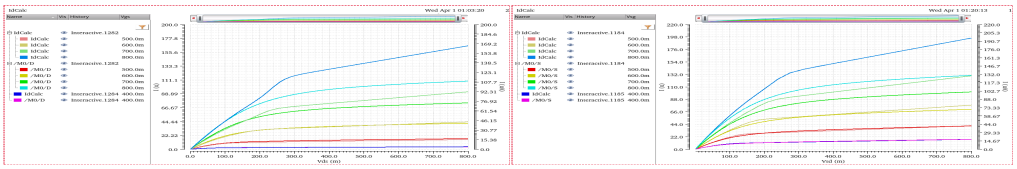
Table 8. FinFET modelling results for Synopsys SAED_PDK14_FinFET®

Device type	Device model parameters		
	V_{T0}[mV]	V_{DS_Sat}[mV]	$K[\mu A/V^2]$
14nm_NCh_HVt	351.37	$V_{DS\_sat} = \frac{V_{GS}}{3}$	1250.67

Device type	Device parameters		
	V_{T0}[mV]	V_{SD_Sat}[mV]	$K[\mu A/V^2]$
14nm_PCh_LVt	227.37	$V_{SD\_sat} = \frac{V_{SG}}{3}$	906.36

Device type	Linear region	
	The coefficient function of V_{T0}, $f_{V_{T0}}(V_{GS})$	The coefficient function of V_{DS}, $f_{V_{DS}}(V_{GS})$
14nm_NCh_HVt	$f_{V_{T0}}(V_{GS}) = 2.\mathbf{13}\|2.\mathbf{17} \cdot V_{GS} + 0.26$	$f_{V_{DS}}(V_{GS}) = -0.70 \cdot V_{GS}^2 + 1.13 \cdot V_{GS} - 0.29$
14nm_PCh_LVt	$f_{V_{T0}}(V_{SG}) = 2.48 \cdot V_{SG} + 0.46$	$f_{V_{SD}}(V_{SG}) = -0.26 \cdot V_{SG}^2 + 0.70 \cdot V_{SG} - 0.09$

Device type	Saturation region equation	Channel length modulation effect, $\lambda(V_{GS})$
14nm_NCh_HVt	$\frac{K}{1.\mathbf{27}\|2.\mathbf{77}}(V_{GS} - V_t)^2 \cdot (1 + \lambda(V_{GS}) \cdot V_{DS})$	$\lambda(V_{GS}) = -12.89 \cdot V_{GS}^3 + 29.50 \cdot V_{GS}^2 - 20.63 \cdot V_{GS} + 5.25$
14nm_PCh_LVt	$\frac{K}{2.80}(V_{SG} - V_t)^2 \cdot (1 + \lambda(V_{SG}) \cdot V_{SD})$	$\lambda(V_{SG}) = -10.71 \cdot V_{SG}^3 + 22.40 \cdot V_{SG}^2 - 14.79 \cdot V_{SG} + 4.04$



(a) Modelling results for 14nm_NCh_HVt (b) Modelling results for 14nm_PCh_LVt

Fig. 9. Original devices characteristics (/M0/D or /M0/S) vs Our model (IdCalc) for SAED14.

Table 9. Relative error between device model, Sah model and proposed model

Device type (GPDK, PTM, SAED14)	Device model vs Sah model	Device model vs Proposed model	Device type (GPDK, PTM, SAED14)	Device model vs Sah model	Device model vs Proposed model
18nm_NCh_HVt	29.42%	0.57%	18nm_PCh_LVt	47.34%	1.14%
18nm_NCh_LSTP	193.82%	3.13%	18nm_PCh_HP	54.45%	2.58%
14nm_NCh_HVt	31.84%	0.40%	14nm_PCh_LVt	39.47%	2.50%

Finally, the functions $f_{V_{T0}}(V_{GS})$ and the saturation equation require calibration only at V_{GS} = 400mV (red constants), whereas they remain valid without correction for $V_{GS} > 400$mV (green constants). In Table 9 the relative error between device model, Sah model and proposed model is presented. As one may observe, poor model accuracy ($\approx$60%) is obtained for the classical Sah-Model, while the proposed model exhibits very high model accuracy ($\geq$97%).

7. Conclusions

A FinFET large signal device model for hand calculation DC analysis was developed using the Cadence Virtuoso® simulation environment and Spectre® simulator and employing the GPDK, PTM and SAED14 models. First-order compact-model parameters such as V_{T0}, K, λ and γ were extracted and a new set of FinFET device equations was proposed in order to improve model accuracy. Equation complexity greatly increased making necessary to use spreadsheet software tools for design space exploration. The proposed model provides valuable hints ($\geq$97% accuracy) regarding circuit operation based on user definable FinFET parameters.

Future work will investigate parameter variations induced by temperature and process corners using Monte Carlo analysis and will examine the small-signal behavior of FinFET transistors. Device matching will also be addressed, subject to the availability of the necessary information.

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